Stability Conditions for a Digital Discrete-Time Non-Foster Circuit Element

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***Abstract*—Digital discrete-time implementations of non-Foster circuit elements offer an alternative to conventional analog circuit approaches. In particular, the design of a discrete-time negative capacitor is investigated, since such non-Foster circuit elements offer significant potential in wideband antenna, metamaterial, and artificial magnetic conductor applications. As with analog non-Foster circuits, stability is an important design consideration for digital non-Foster elements. Therefore, stability conditions and simulation results are presented for a discrete-time negative capacitor, and the onset of instability is shown near the predicted stability boundary.**

I. Introduction

Digital discrete-time implementations of non-Foster circuits such as negative capacitors and negative inductors provide an important alternative to analog approaches [1], [2]. These non-Foster circuit elements can be used to improve performance in important emerging technologies such as artificial magnetic conductors, microwave metamaterials, and electrically-small antennas [3]–[5]. However, stability issues are of practical concern in the design of such circuits [6]. While digital non-Foster circuits may be less susceptible to component variations, stability remains an important design consideration.

To illustrate the stability analysis of digital discrete-time non-Foster circuit elements, consider the system of Fig. 1 where an ADC (analog-to-digital converter) first converts continuous-time voltage $v_{in}(t)$ into discrete-time signal $v_{in}[n] = v_{in}(nT)$ for sampling period T. The digital signal processing consists of the convolution $i_{in}[n] = h[n] * v_{in}[n]$, where the z-transform of $h[n]$ is $H(z) = \mathcal{Z}\{h[n]\}$. Finally, $i_{in}[n]$ is converted into the continuous-time input current $i_{in}(t)$ by the DAC (digital-to-analog converter), typically with an implied ZOH (zero-order hold). In addition, the current source $i_s(t)$ with source resistance R_s drives the non-Foster circuit element on the right of Fig. 1.

The Laplace transform of input terminal current $i_{in}(t)$ is $I_{in}(s) = V^\star(s)H(z)(1-z^{-1})/s\big|_{z=e^{sT}}$, assuming a zero-order hold in the DAC, and where $V^\star(s) = \sum v(nT)e^{-nsT}$, for integer n, is the starred transform [7]. The impedance of the non-Foster element of Fig. 1 is then [1], [2]

$$Z(s) = \frac{V_{in}(s)}{I_{in}(s)} \approx \frac{sT}{[(1-z^{-1})H(z)]}\bigg|_{z=e^{sT}}, \qquad (1)$$

for $v_{in}(t)$ sampled without aliasing and frequencies below $0.5/T$ Hz. The stability of Fig. 1 can then analyzed in terms of the terminal input current $i_{in}(t)$ that results from excitation by signal source $i_s(t)$. Since $v_{in}(t) = R_s[i_s(t) - i_{in}(t)]$, the system transfer function $G(s)$ can be written as

$$G(s) = \frac{I_{in}(s)}{I_s(s)} \approx \frac{R_s H(z)}{1 + R_s H(z)}\bigg|_{z=e^{sT}}, \qquad (2)$$

for $v_{in}(t)$ sampled without aliasing and frequencies below $0.5/T$ Hz. Finally, the system in Fig. 1 is stable if the poles of the corresponding discrete-time transfer function $G(z)$ are inside the unit circle [7]:

$$G(z) = \frac{R_s H(z)}{1 + R_s H(z)}. \qquad (3)$$

II. A Discrete-Time Negative Capacitor

As a simple illustration, a negative (or positive) capacitor with continuous-time relation $i(t) = Cdv(t)/dt$ can be roughly approximated by the discrete-time equivalent $i_{in}[n] = C(v_{in}[n] - v_{in}[n-1])/T$, and having z-transform $I_{in}(z) = C(1-z^{-1})V_{in}(z)/T$. Denoting the transfer function $H(z)$ in Fig. 1 for a negative capacitor as $H_C(z)$, a capacitor can thus be implemented with $H_C(z) = C(1-z^{-1})/T$, where T is the clock period for the ADC and DAC, C is the design capacitance, and C can be either positive or negative. The

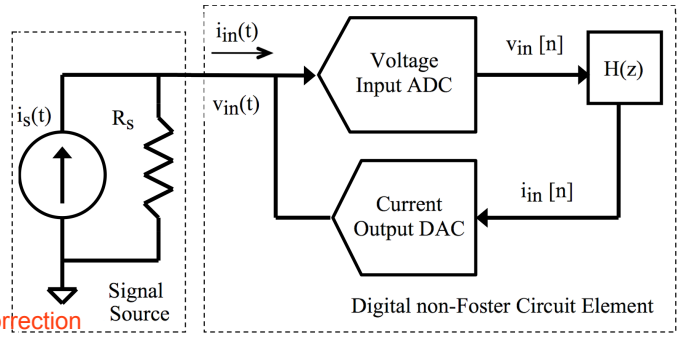

Fig. 1. Block diagram of a digital discrete-time non-Foster circuit element driven by external current source $i_s(t)$ with source resistance R_s [1], [2]. The input voltage is converted by the ADC into discrete-time signal $v_{in}[n] = v_{in}(nT)$ and processed by a discrete-time filter with z-transform $H(z)$. Input current $i_{in}(t)$ is generated by the DAC from filter output $i_{in}[n] = h[n] * v_{in}[n]$, where the ADC and DAC have high impedance and clock period T.

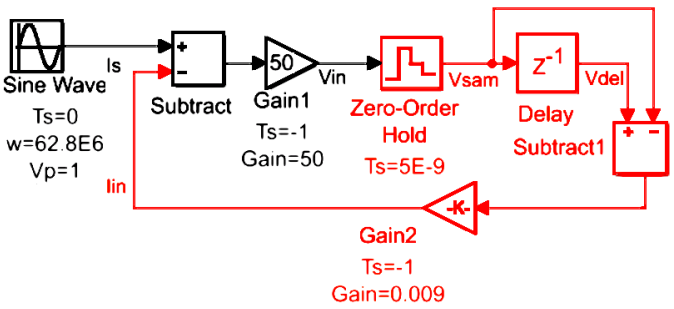

Fig. 2. MathWorks Simulink model of a negative capacitor implementation of the system of Fig. 1 with $C = -45$ pF, with $H_C(z) = C(1-z^{-1})/T = -0.009(1-z^{-1})$, and with a 10 MHz external current source [1]. The black blocks are continuous-time models, and red blocks are discrete-time with sample period $T = 5$ ns.

overall system transfer function from (3) is then denoted $G_C(z)$ for the capacitor:

$$G_C(z) = \frac{R_sC(1-z^{-1})}{T + R_sC(1-z^{-1})} = \frac{(z-1)}{z\left(1+\frac{T}{R_sC}\right)-1}, \qquad (4)$$

for $v_{in}(t)$ sampled without aliasing and frequencies below $0.5/T$ Hz. Since (4) has a single pole at $z = 1/[1+T/(R_sC)]$, this pole establishes the stability conditions for the positive or negative capacitor, and the design is stable when:

$$T/(R_sC) < -2 \quad \text{or} \quad T/(R_sC) > 0\,. \qquad (5)$$

The design of a negative capacitor implementation of Fig. 1 is shown in Fig. 2. Here, the signals I_s, V_{in}, and I_{in}, in Fig. 2 correspond to the signals $i_s(t)$, $v_{in}(t)$, and $i_{in}(t)$ in Fig. 1, respectively. The gain of block Gain1 corresponds to source resistance $R_s = 50\,\Omega$ in Fig. 1, such that $v_{in}(t) = 50[i_s(t) - i_{in}(t)]$. Blocks Sine Wave, Subtract, and Gain1 in Fig. 2 are continuous-time models, while the remaining red blocks are discrete time models with sample period $T = 5$ ns. As shown, $H_C(z) = C(1-z^{-1})/T = -0.009(1-z^{-1})$, so $C = -45$ pF.

For the $C = -45$ pF design of Fig. 2, Keysight ADS large-signal S-parameter simulation was used to verify the predicted impedance, as shown in Fig. 3, and as further described in [2]. The solid red curve is the real part of input impedance $Z(s)$, and the dashed blue curve is the imaginary part. The predicted impedance is $+j354$ ohms for -45 pF at 10 MHz, and the observed impedance is $-101 + j349$ ohms at 10 MHz.

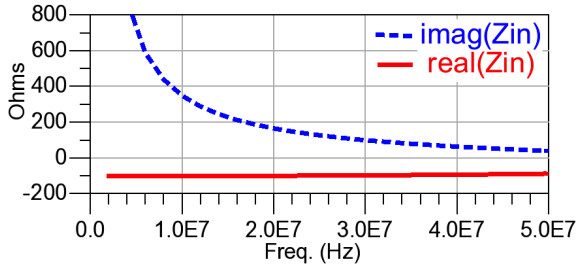

Fig. 3. Keysight ADS large-signal S-parameter simulation results for system of Fig. 2 with $T = 5$ ns and $C = -45$ pF [1]. The solid red curve is the real part of input impedance $Z(s)$, and dashed blue curve is the imaginary part. The predicted impedance is $+j354$ ohms for -45 pF at 10 MHz, and the observed impedance is $-101 + j349$ ohms at 10 MHz.

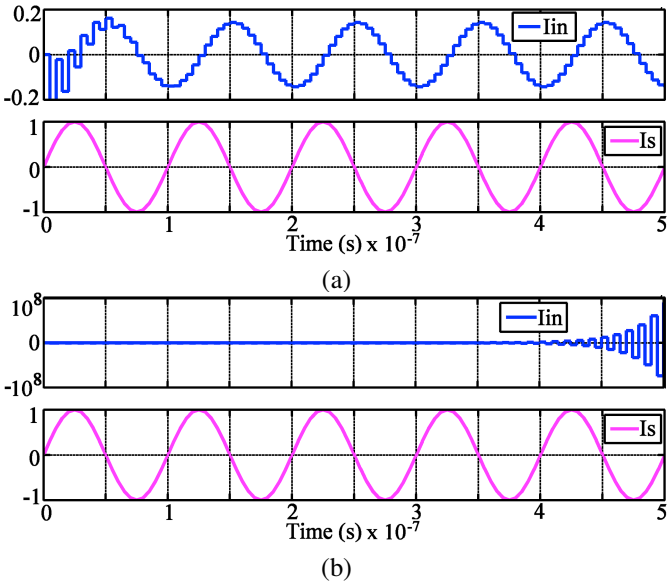

Fig. 4. MathWorks Simulink simulation results [1]. (a) Stable system results for system of Fig. 2, implementing a negative capacitance of $C = -45$ pF, with Gain2 set to 0.009 such that $H_C(z) = C(1-z^{-1})/T = -0.009(1-z^{-1})$, and (5) is satisfied with $T/(R_sC) = -2.22 < -2$. (b) Unstable results for system of Fig. 2, with Gain2 set to 0.011, $C = -55$ pF, with $H_C(z) = -0.011(1-z^{-1})$, so (5) is *not satisfied* with $T/(R_sC) = -1.82$.

(Note that further theory on the underlying mechanism and mitigation of the resistive component of $Z(s)$ is given in [2].)

For the $C = -45$ pF design of Fig. 2, stable MathWorks Simulink simulation results results are shown in Fig. 4(a), where Gain2 is set to 0.009, and the predicted stable pole is inside the unit circle at $z = 1/[1+T/(R_sC)] = 1/[1-2.22] = -0.82$. Unstable system results are shown in Fig. 4(b), where Gain2 is set to 0.011, and the system is just beyond the stability boundary of (5), with $T/(R_sC) = -1.82$, and with an unstable pole at $z = -1.22$. Results in Fig. 4(b) are clearly unstable with current in excess of 10^8 A.

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