Parasitic Resistance in Non-Foster Circuits Caused by Current Conveyor Frequency Response

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***Abstract*—Current conveyors are useful for creating non-Foster circuit components such as negative capacitors. As with operational amplifiers, it is sometimes desirable to use phase compensation techniques to improve the phase margin and stability in these circuits. However, it is shown for negative capacitor applications that the frequency response in a current conveyor leads to undesired parasitic resistance and reduced quality factor, Q. Analysis of the circuit shows that current conveyor frequency response can cause such degraded performance. In addition, measured data for a CMOS implementation confirm the predicted deleterious effects of current conveyor frequency response on parasitic resistance and quality factor.**

***Keywords*—current mode circuits, frequency response.**

I. Introduction

Current conveyors are useful in a variety of applications where current is to be conveyed between input and output impedances that are very different. They were first proposed in 1968, and the second-generation designs were proposed in 1970 [1]. In more advanced current conveyor implementations, the addition of frequency compensation networks can improve stability by using techniques similar to those used in operational amplifiers [2]–[4]. In some current conveyor applications, however, the frequency response can also have significant adverse effects on performance of the overall circuit.

When current conveyors are used to implement certain non-Foster circuits such as a negative capacitor, the current conveyor frequency response can lead to degraded quality factor, Q [5]–[8]. In the following, it is shown that there is a relationship between the frequency response of the circuit and an accompanying induced parasitic resistance that degrades Q. In Section II, theory is provided relating current conveyor frequency response to Q of a negative capacitor circuit. In Section III, a CMOS implementation of the circuit is given along with simulation results. In Section IV, measured results for a CMOS implementation of a negative capacitor confirm the predicted behavior.

II. Circuit Analysis

Fig. 1 shows a simplified diagram of a second-generation current conveyor (CCII). For an ideal CCII+ current conveyor, the following relations should be true:

$$i_x = i_z, \tag{1}$$

$$V_x = V_y, \tag{2}$$

and

$$i_y = 0. \tag{3}$$

Ideally, $i_z/i_x = 1$ and $V_x/V_y = 1$. However, any practical implementation of a current conveyor entails some bandwidth limitation and accompanying frequency response. For a practical current conveyor circuit, (2) will not be constant at all frequencies, and a single-pole frequency-domain model $A(s)$ model would be:

$$V_x = A(s)V_y, \tag{4}$$

with

$$A(s) = \frac{1}{1 + j\frac{\omega}{\omega_0}}, \tag{5}$$

where w_0 is the 3 dB frequency. Typically, $A(s)$ and the 3 dB bandwidth of the current conveyor are adjusted for stability using internal compensation [4].

To observe the effect of current conveyor frequency response in degrading quality factor, consider the circuit in Fig. 2. In this figure, a CCII+ current conveyor is connected in a Negative Impedance Converter (NIC) configuration. For this circuit, the input impedance Z_{IN} is

$$Z_{IN} = \frac{V_y}{i_z}\ . \tag{6}$$

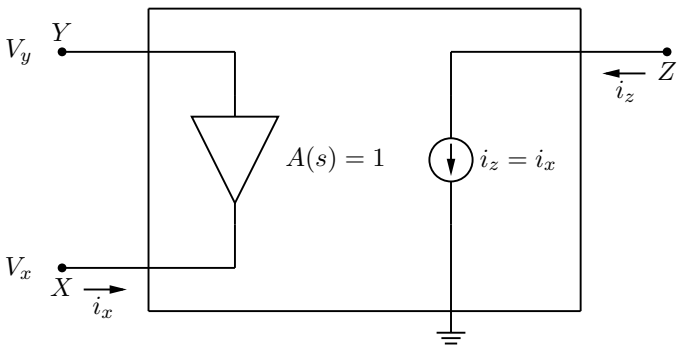

Fig. 1: Simplified model of a current conveyor.

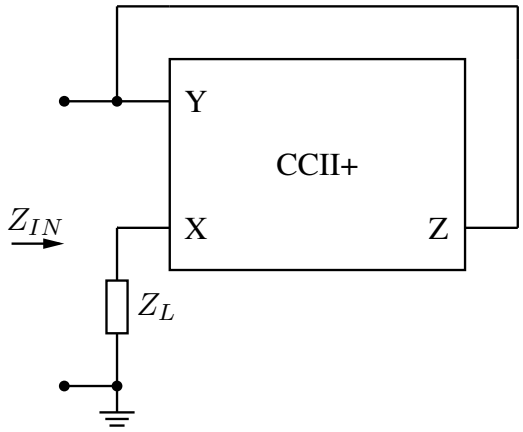

Fig. 2: Current-conveyor NIC application.

but $i_x = i_z$, so

$$Z_{IN} = \frac{V_y}{i_x} , \tag{7}$$

and $V_y = V_x/A(s)$, so

$$Z_{IN} = \frac{V_x}{i_x A(s)} , \tag{8}$$

and, since $Z_L = -V_x/i_x$,

$$Z_{IN} = -\frac{Z_L}{A(s)} = -Z_L \left(1 + j\frac{\omega}{\omega_0}\right) . \tag{9}$$

For the circuit in Fig. 2, when Z_L is a capacitor, the input impedance Z_{IN} becomes a negative capacitance. In this case, (9) becomes

$$Z_{IN} = \frac{j}{\omega C}\left(1 + j\frac{\omega}{\omega_0}\right) = \frac{j}{\omega C} - \frac{1}{\omega_0 C} , \tag{10}$$

where it is important to note that the resistive term arises from the frequency response of $A(s)$, without any resistive components in the circuit. Q becomes

$$Q = \left|\frac{\mathrm{Im}(Z_{IN})}{\mathrm{Re}(Z_{IN})}\right| = \frac{\frac{1}{\omega C}}{\frac{1}{\omega_0 C}} = \frac{\omega_0}{\omega}. \tag{11}$$

Thus, the predicted Q of the negative capacitance circuit of Fig. 2 is $Q = 1$ at the 3 dB frequency of $A(s)$, when $\omega = \omega_0$.

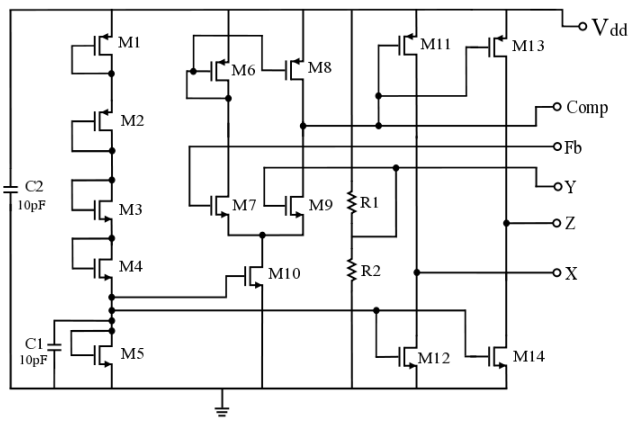

Fig. 3: Current conveyor schematic.

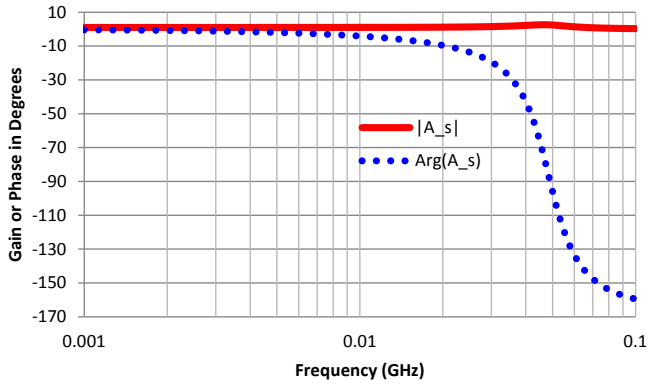

Fig. 4: Simulated magnitude (solid red curve) and phase (dotted blue curve) of $A(s)$ for the current conveyor circuit. The phase is $-45°$ at 42 MHz.

III. Simulation Results

A CMOS current conveyor design is shown in Fig. 3 [9]. In this circuit, transistors M1-M5 provide bias, M6-M10 is the gain stage, and M11-M14 are current mirrors used to provide inputs X and Z. Conventional RC feedback compensation methods between pins *Comp* and *X* assure stability and control phase margin. The circuit of Fig. 2 was configured as a -52 pF negative capacitor using a 52 pF load for Z_L, and then simulated in Agilent ADS.

Fig. 4 shows the simulated magnitude (solid red curve) and phase (dotted blue curve) plots for $A(s)$. The phase is $-45°$ at approximately 42 MHz. Fig. 5 shows the simulated impedance,

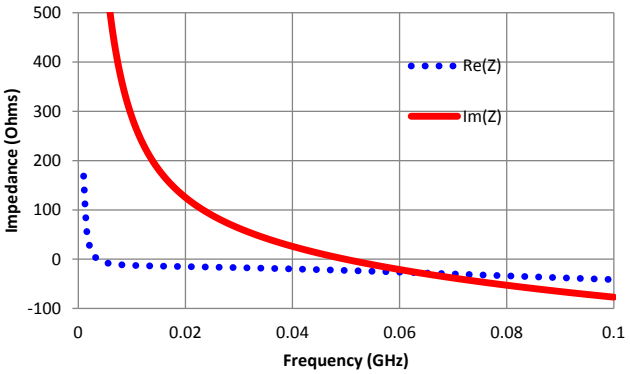

Fig. 5: Simulated impedance plots for the current conveyor circuit, with the reactance $\mathrm{Im}(Z_{IN})$ in solid red and with resistance $\mathrm{Re}(Z_{IN})$ in dotted blue.

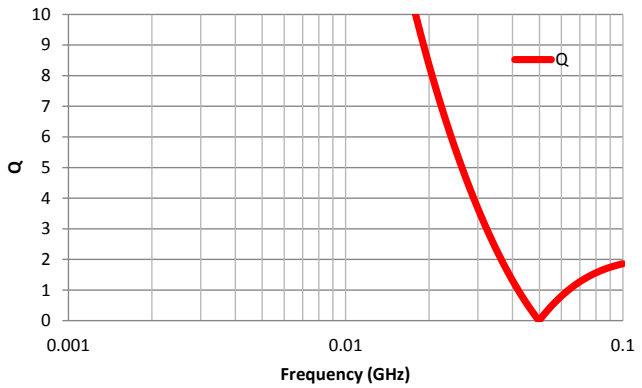

Fig. 6: Simulated Q plot for the current conveyor circuit. In this case, $Q = 1$ at 42 MHz.

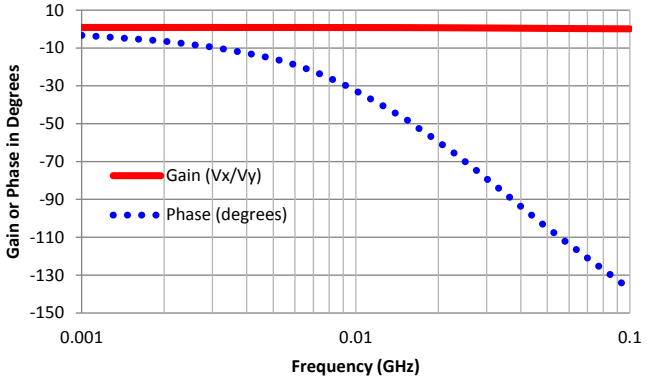

Fig. 8: Measured magnitude (solid red curve) and phase (dotted blue curve) of $A(s)$ for the current conveyor circuit. The phase is $-45°$ at 14 MHz.

with the reactance Im(Z_{IN}) in solid red and with resistance Re(Z_{IN}) in dotted blue. Clearly, the reactance is that of a negative capacitor at low frequency, with sign opposite that of a positive capacitor. Fig. 6 shows the simulated Q. As predicted, the resistance and reactance are of equal magnitude at 42 MHz, and the observed quality factor is $Q = 1$. Thus, the frequency response of $A(s)$ in the current conveyor is observed to induce the predicted resistive component in input impedance Z_{IN} and predicted quality factor Q.

IV. Measurement Results

The circuit from Fig. 3 was fabricated in a 0.5 μm CMOS process, and the fabricated circuit is shown in Fig. 7. The circuit's performance for a 52 pF external load for Z_L was measured using a vector network analyzer. The measured gain (solid red curve) and phase (dotted blue curve) is shown in Fig. 8. The measured impedance is shown in Fig. 9 with the reactance Im(Z_{IN}) in solid red and with resistance Re(Z_{IN}) in dotted blue. The resulting Q is shown in Fig. 10. At 10.9 MHz, the measured quality factor is $Q = 1$, and the measured phase is $-35.6°$, very near the predicted $-45°$ phase shift for $Q = 1$. Package and printed circuit board parasitic capacitances and process variance are suspected to have contributed to the decreased bandwidth observed in the measured circuit, in addition to poles beyond the dominant pole in the simple model in (9). Nevertheless, the measured phase and measured Q correspond well with the predicted relationship of $Q = 1$ at phase of $-45°$.

V. Conclusion

A negative capacitor using a current conveyor was analyzed, simulated, fabricated in 0.5 μm CMOS, and measured. The simulation and measurements show that the frequency response of the current conveyor has a direct influence on the parasitic resistance and Q of the circuit. Results show that when the phase of the gain stage is $-45°$ in a first-order model, then $Q = 1$ and the parasitic resistance will be of the same magnitude as the reactance. More generally, the frequency response of the current conveyor was shown to affect the parasitic resistance exhibited by the circuit.

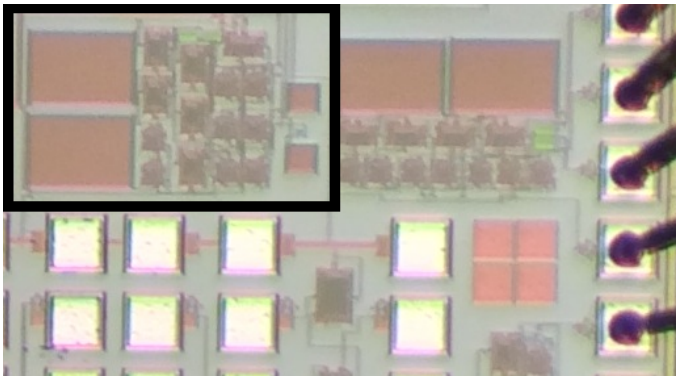

Fig. 7: Photograph of current conveyor circuit with black box showing the location of the circuit.

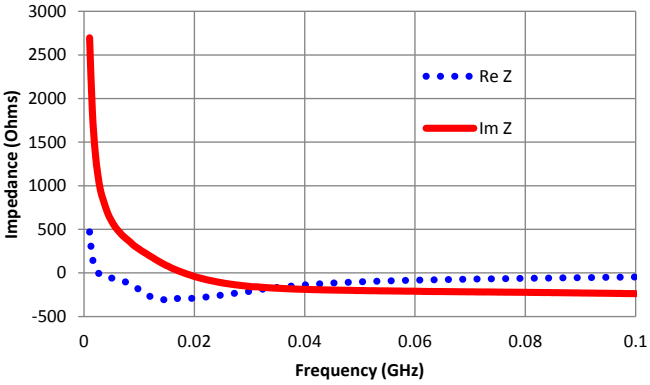

Fig. 9: Measured impedance of the current conveyor circuit, with the reactance Im(Z_{IN}) in solid red and with resistance Re(Z_{IN}) in dotted blue..

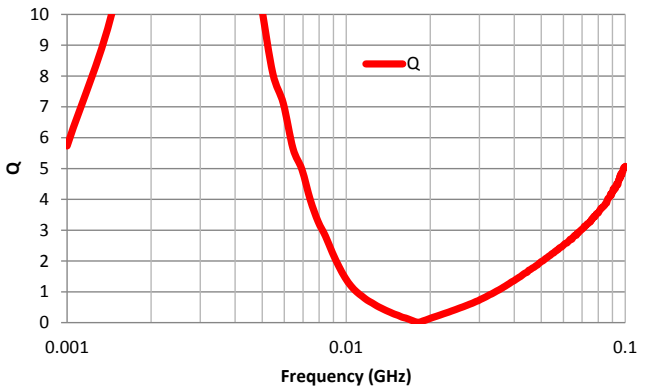

Fig. 10: Measured Q plot for the current conveyor. In this case, $Q = 1$ at 10.9 MHz.

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