Measurement of a CMOS Negative Inductor for Wideband Non-Foster Metamaterials

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***Abstract*—There is increasing interest in impedance-matching methods that use non-Foster circuits to provide wideband operation in a variety of microwave devices such as antennas and metamaterials. In addition, many of these prior non-Foster circuits employ bipolar negative impedance converter designs, and it is advantageous to move such designs into CMOS. Therefore, the present work provides new measured results building upon an earlier proposed design of a negative inductor in a 0.5 micron CMOS process. The proposed circuit eliminates a resistor from a common negative impedance converter topology, and the prototype performs well at high frequency. Measured results show a low-frequency inductance of -95 nH falling to -85 nH at 750 MHz and -63 nH at 1 GHz. Finally, simulation results are presented for the performance of the circuit in a metamaterial application.**

***Keywords*—metamaterials, impedance matching, CMOS integrated circuits.**

I. Introduction

Emerging technologies such as cognitive radio systems require frequency agility over wide portions of the spectrum in order to coexist with other spectrum users [1]. This, in turn, has driven the investigation and development of a number of new approaches to a variety of devices and components such as non-Foster wideband antennas, non-Foster artificial magnetic conductors, and non-Foster metamaterial approaches [1]–[6]. In this, non-Foster elements such as negative capacitors and negative inductors are commonly used to eliminate narrowband resonant behavior inherent to the devices. Such circuits can be used effectively to improve impedance matching when compared to matching using passive networks [4]. In addition, many of these earlier non-Foster circuits employ bipolar negative impedance converter designs, and industry trends for system-on-a-chip designs motivate the development of CMOS circuit approaches.

To address this opportunity, a novel CMOS negative inductor design is presented where a common circuit topology is modified and good high-frequency performance is observed. In the proposed approach, a resistor is eliminated from a CMOS implementation of a common bipolar Linvill negative impedance converter topology [7], [8]. The proposed circuit was fabricated in 0.5 μm CMOS to demonstrate the proposed design. More advanced CMOS processes would, of course, be expected to extend performance to higher frequencies. Measurements of the fabricated CMOS prototype show good performance at high frequency and good agreement with theoretical results. Simulation results are also provided showing performance of the circuit in a metamaterial application.

In Section II, the theoretical analysis of the proposed CMOS negative inductor circuit are reviewed. In Section III, simulation results in Agilent ADS are shown along with measured results for the prototype circuit fabricated in 0.5 μm CMOS, and simulated performance in a metamaterial.

II. Proposed Circuit and Analysis

The proposed circuit is a modified CMOS version of the grounded negative inductor based on the Linvill SCS negative inductor design [7] following prior results [9]. In the proposed CMOS circuit of Fig. 1, the negative inductance is seen at the input port impedance Z_i, at the drain of nMOS transistor M_2, with the source of M_2 grounded ($R_1 = 0$). The gate of pMOS transistor M_1 also connects to the input port, with its drain connected to ground through bias resistor R_L in parallel with load impedance Z_L, and with its source connected to supply voltage V_{DD} through resistor R_2. The proposed CMOS circuit shown in Fig. 1 differs from more common implementations by omitting one resistor (setting $R_1 = 0$) and using MOSFET internal capacitances to make up the capacitive part of the load Z_L, so no separate capacitor component is used.

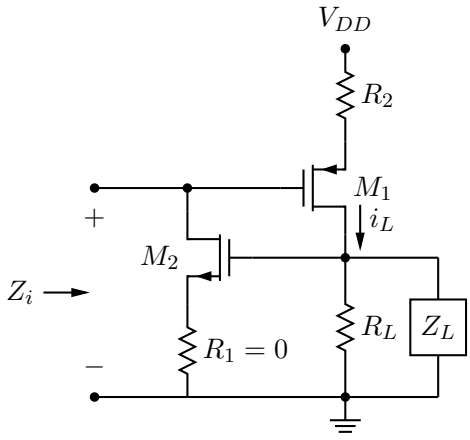

Fig. 1. Schematic of proposed CMOS negative inductance circuit.

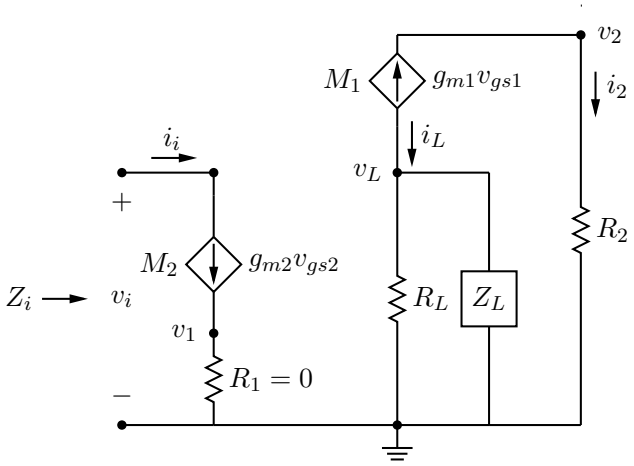

Fig. 2. Small-signal model.

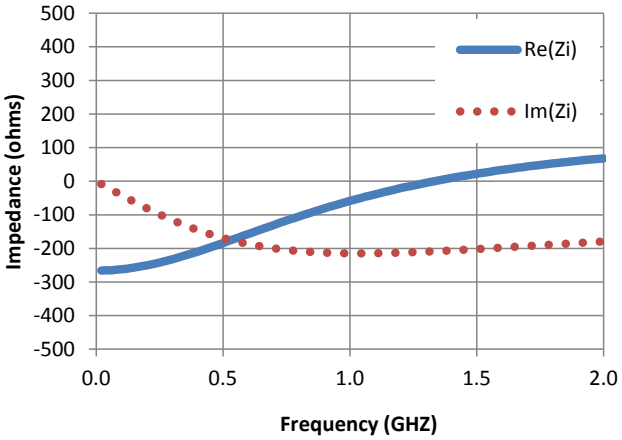

Fig. 3. Simulation results showing real part of Z_i (solid blue) and imaginary part of Z_i (dotted red).

The small-signal model for the circuit of Fig. 1 is shown in Fig. 2. To simplify the analysis, Z'_L is introduced, where $Z'_L = R_L||Z_L$. Then, the voltage equations for the circuit are given as [9]:

$$v_{gs1} = v_i - v_2 \ , \tag{1}$$

and

$$v_{gs2} = v_L - v_1, \tag{2}$$

where v_{gs1} and v_{gs2} are the gate-source voltages of transistors M_1 and M_2. Since $R_1 = 0$ for this circuit, $v_1 = 0$ so $v_{gs2} = v_L$. Also,

$$v_2 = i_2 R_2 = -i_L R_2. \tag{3}$$

The equations for the circuit currents are then:

$$i_i = g_{m2} v_L \ , \tag{4}$$

and

$$i_L = -i_2 = -g_{m1}(v_i - v_2). \tag{5}$$

The input impedance is $Z_i = v_i/i_i$, so from (4) the next step is to solve for v_L in terms of the input voltage and the circuit parameters. By substituting for i_L from (3) and (5),

$$v_L = i_L Z'_L = -g_{m1}(v_i - v_2)Z'_L = -g_{m1}(v_i + i_L R_2)Z'_L, \tag{6}$$

$$v_L = -g_{m1}\left(v_i + \frac{v_L}{Z'_L}R_2\right)Z'_L = -g_{m1}(v_i Z'_L + v_L R_2). \tag{7}$$

Combining terms and solving for v_L gives

$$v_L(1 + g_{m1}R_2) = -g_{m1} v_i Z'_L, \tag{8}$$

$$v_L = \frac{-g_{m1} v_i Z'_L}{1 + g_{m1}R_2}. \tag{9}$$

Substituting this for v_L in (4),

$$i_i = g_{m2}\frac{-g_{m1} v_i Z'_L}{1 + g_{m1}R_2}. \tag{10}$$

Z_i can now be found by substituting this for i_i,

$$Z_i = \frac{v_i}{i_i} = \frac{1 + g_{m1}R_2}{g_{m1}g_{m2}}\left(\frac{-1}{Z'_L}\right). \tag{11}$$

Expanding Z'_L this becomes [9]

$$Z_i = \frac{1 + g_{m1}R_2}{g_{m1}g_{m2}}\left(-\frac{1}{R_L} - \frac{1}{Z_L}\right). \tag{12}$$

The current prototype of the circuit used values of $R_2 = R_L = 1000\ \Omega$, pMOS transistor M_1 with width×length of 100×0.5 μm and nMOS transistor M_2 of 50×0.5 μm. This results in values of $g_{m1} = 0.0043$ S at 1.74 mA, and $g_{m2} = 0.0055$ S at 4.96 mA. So,

$$Z_i = 224000\left(-\frac{1}{R_L} - \frac{1}{Z_L}\right) = -224 + 224000\ j\omega C, \tag{13}$$

where $Z_L = 1/j\omega C$, and C is the load capacitance comprised of the parasitic capacitance of the two transistors, and was estimated to be $C = 0.228$ pF, so this becomes

$$Z_i = -224 + j\omega \cdot 51 \text{ nH}. \tag{14}$$

III. Measured and Simulated Results

The circuit was simulated in Agilent ADS, with real and imaginary parts of input impedance Z_i shown in Fig. 3 and

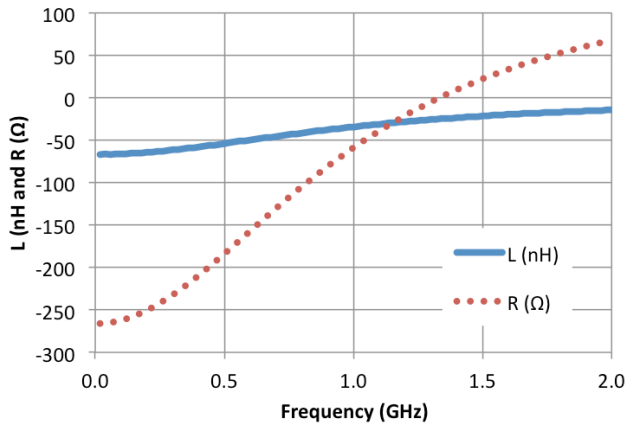

Fig. 4. Simulation results showing extracted inductance L in nH (solid blue) and resistance R in ohms (dotted red).

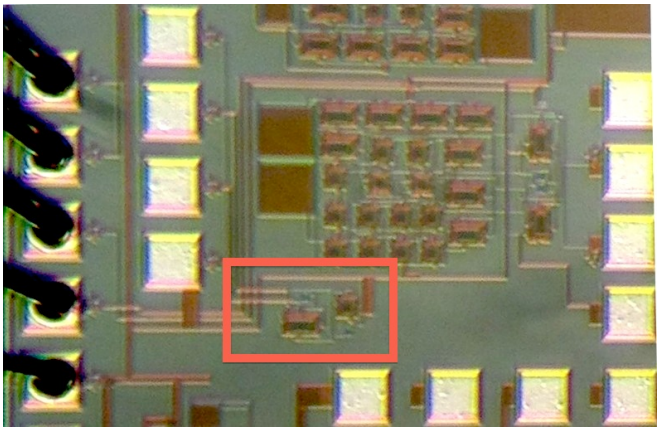

Fig. 5. Photograph of prototype negative inductance circuit with red box showing location of the circuit of Fig. 1.

the extracted inductance and resistance shown in Fig. 4. The negative inductance is evident in the downward trajectory of the imaginary part of Z_i at low frequencies in Fig. 3, and corresponds to a negative inductance of -65 nH, shown in Fig. 4.

In addition, a negative resistance of $-260\ \Omega$ was observed at low frequency. Such negative resistance may be desirable for gain in some applications or may be mitigated with positive resistance in other applications.

The fabricated circuit is shown in Fig. 5 and was measured using an S-parameter network analyzer with a bias tee providing dc bias for the circuit. The measured results were used to plot the negative inductance and resistance as shown in Fig. 6. The negative inductance is observed to be fairly constant through 700 MHz, and the resistance remains negative through 1 GHz.

A Smith chart showing measured S11 corresponding to the impedance seen at input port Z_i is shown in Fig. 7. As expected, the plot is outside of the normal Smith chart due to the negative resistance component of Z_i, as seen in Fig. 3 and Fig. 6.

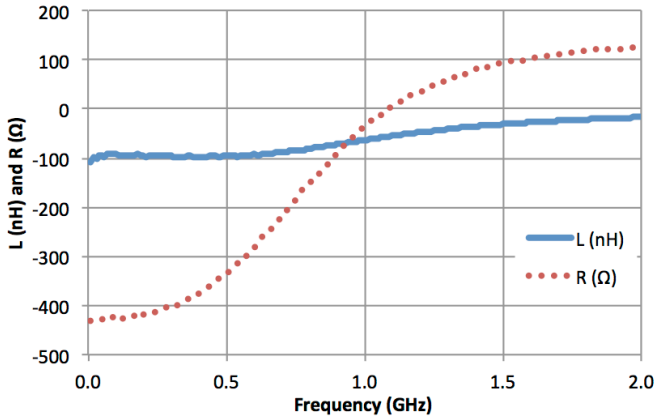

Fig. 6. Data for prototype circuit showing measured inductance L in nH (solid blue) and measured resistance R in ohms (dotted red).

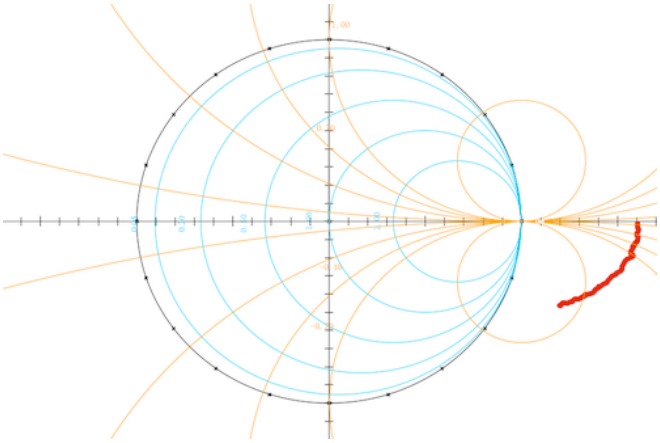

Fig. 7. Smith chart showing measured S11 of input impedance Z_i.

As shown in Fig. 4, the simulated response of the circuit includes both a negative capacitance and a negative series resistance. This series resistance might affect the performance of metamaterials that utilize this circuit. To show this effect, the split ring resonator (SRR) shown in Fig. 8 was simulated twice, once with ideal ($R = 0$) loading, and once with non-ideal ($|R| > 0$) loading.

The split ring resonator shown in Fig. 8 has an outer radius of 32 mm, and a capacitive gap of 2.5 mm. The structure was simulated in an ideal parallel plate waveguide, where the top and bottom plates were defined as perfect electrical conductor (PEC) boundaries, and were spaced 50 mm apart. The side plates were defined as perfect magnetic

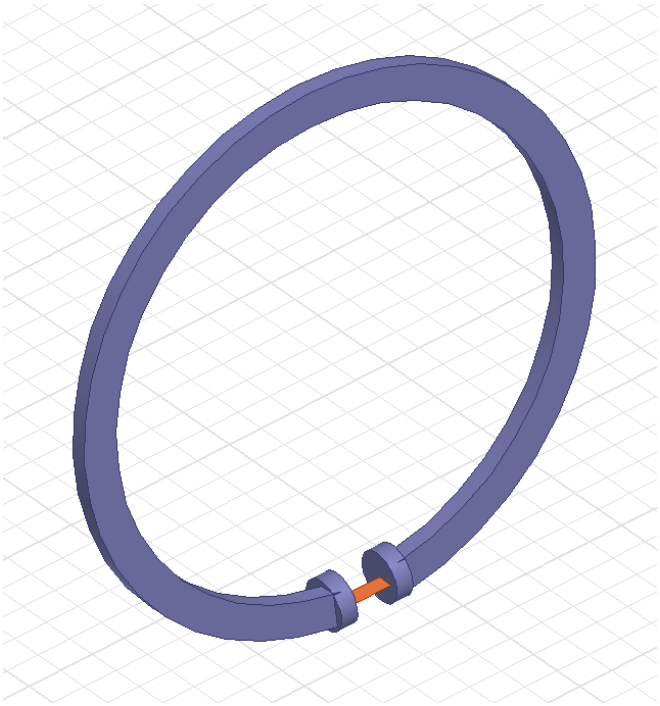

Fig. 8. SRR simulated with both ideal and non-ideal non-Foster loading.

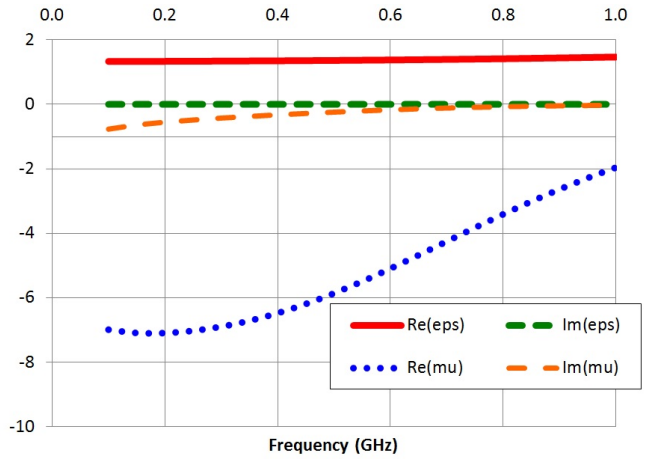

Fig. 9. Extracted real and imaginary parts of permeability and permittivity, for the ideal case where R=0.

conductor (PMC) boundaries, and were spaced 40 mm apart. The first simulation was of the SRR with a capacitive load of $C = -225$ fF in parallel with an inductive load of $L = -55$ nH, with no resistive loading along the lines of [10]. Fig. 9 shows the extracted real and imaginary parts of the simulated permeability and permittivity resulting from this load [11]. The second simulation was of the SRR with a capacitive load of $C = -225$ fF in parallel with an RL series combination where $L = -55$ nH and $R = -240\ \Omega$. These loading values were chosen to approximately match the simulated data shown in Fig. 4. The extracted permeability and permittivity resulting from this simulation are shown in Fig. 10. As can be seen, the addition of the series resistance eliminated the desired negative permeability response.

IV. Conclusion

A simple two-transistor negative inductor has been analyzed, simulated, measured and fabricated in $0.5\ \mu$m CMOS. The measured negative inductance values compared favorably the analysis and simulation. The estimated Z_i was $-224 + j\omega \cdot 51$ nH, the simulation yields $-265 + j\omega \cdot 66$ nH, and the measured values yield $-425\ \Omega + j\omega \cdot 95$ nH. The circuit showed stability and consistent results through 1 GHz.

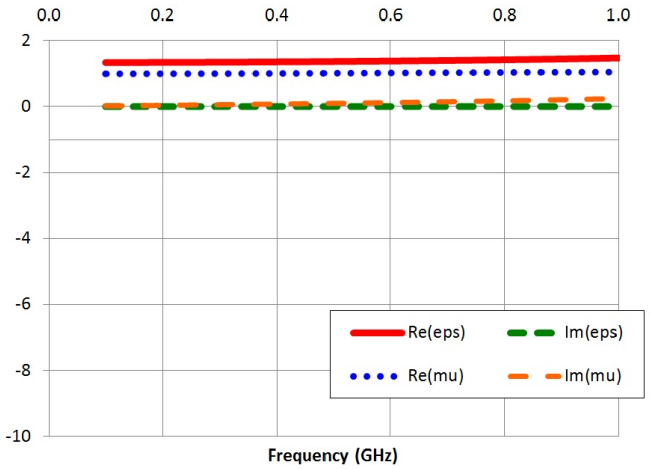

Fig. 10. Extracted real and imaginary parts of permeability and permittivity, for the real case where $R = -240\ \Omega$.

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