Measurement and Simulation of a CMOS Current Conveyor Negative Capacitor for Metamaterials

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Abstract— **Current conveyors can be used as building blocks for implementing non-Foster circuits such as negative capacitors and negative inductors that are useful in extending bandwidth in metamaterials. In the present paper, measured results are presented for a prototype integrated circuit current conveyor negative capacitor. This circuit has been fabricated in a 0.5 micron CMOS process following previous results. Although CMOS is a desirable technology for circuit implementation, it is accompanied by design challenges of associated parasitic resistance. To investigate these issues, a prototype second generation current conveyor (CCII) is designed and tested in a negative capacitance circuit. In addition, full-wave electromagnetic simulation results are also presented showing the effects of observed resistance on overall metamaterial performance.**

Keywords— negative capacitance; metamaterials; CMOS; non-Foster; second generation current conveyor (CCII+).

I. INTRODUCTION

There has been an impressive advancement in the architecture of current conveyors since their introduction in 1968, followed by the reformulation by Sedra and Smith in 1970 [1], [2]. Current conveyors can be used to implement active filter designs, instrumentation applications and signal processing applications [3]-[7]. Furthermore, current conveyors can also be used to implement non-Foster circuits in metamaterial applications to partially overcome the limitations on bandwidth and gain characteristics [8].

The reactance or susceptance of typical circuit elements, such as inductors and capacitors monotonically increases with frequency. On the other hand, non-Foster circuits can violate this principle. Although non-Foster elements have long been present in the literature, their applications remain limited. This may be, in part, due to the fact that CMOS implementations of non-Foster elements can suffer from unwanted parasitic resistance [9] – [11]. Therefore, the present paper considers the design of a second generation current conveyor in a 0.5 micron CMOS process specifically for use in wideband metamaterial applications. Furthermore, the effect of such parasitic resistance on metamaterial structures is investigated.

The proposed circuit has been fabricated in 0.5 micron CMOS and tested, following earlier designs in [12]. Among the different type of current conveyors available, they are mainly classified into three generations. This paper focuses on a second generation current conveyor (CCII), which belongs to the emerging class of high performance analog circuit design based on current-mode approach making it ideal for designing analog circuits that can be integrated on a single chip[13]-[16].

In the following sections, the detailed design of a second-generation CMOS current conveyor is described and its attribute of impedance inversion is analyzed. The subsequent section show the simulation results. The following section considers the effect of parasitic resistance of a non-ideal negative capacitor on metamaterial structures. Finally measured results of a negative capacitance circuit are presented.

II. CIRCUIT ANALYSIS

The second generation current conveyor (CCII) measured in this paper follows earlier design considerations from [12]. Typically a CCII is a three-port device as shown in the box inset of Fig. 1, with a high impedance input port to avoid loading effects. The matrix equivalent of the second
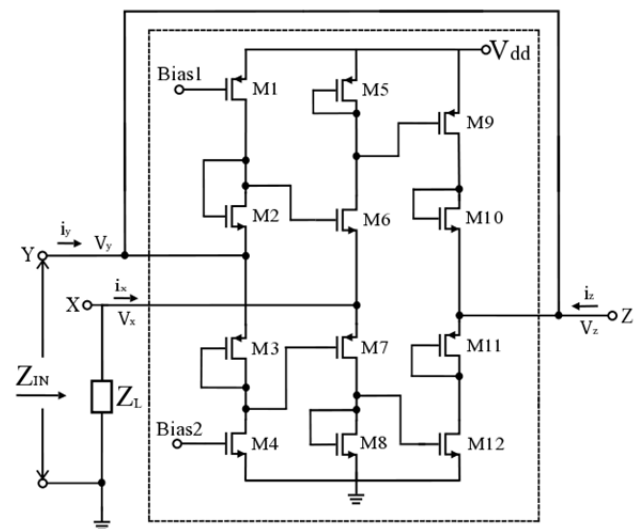

Fig. 1. Detailed schematic of a negative impedance converter. The second generation current conveyor circuit (CCII+) is shown in inset box.
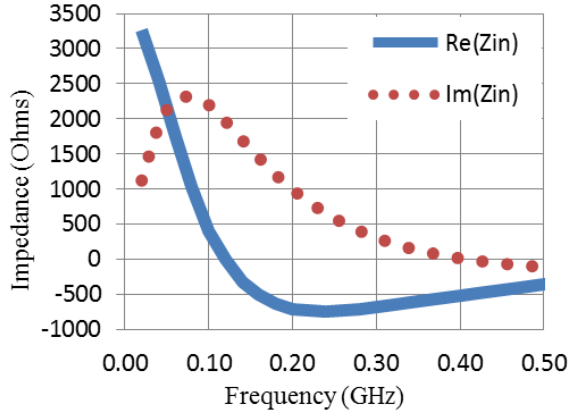
Fig. 2. Simulation results showing input impedance Z_{in} with real part (solid blue) and imaginary part (dotted red) for a 1.3 pF load capacitor Z_L for the circuit in Fig. 1.

generation current conveyor is given as:

$$\begin{pmatrix} i_y \\ v_x \\ i_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} v_y \\ i_x \\ v_z \end{pmatrix} \qquad (1)$$

where the subscripts x, y and z, refer to the voltages and currents at terminals labelled X, Y and Z in the box inset of Fig. 1. Ideally, there is no current flow into the Y terminal. As a result, terminal Y exhibits infinite input impedance. Also, the voltage at terminal X equals the voltage applied to terminal Y, and the terminal X exhibits zero input impedance. The $\pm$ sign sets the flow of current between the X and Z terminals in same or opposite direction respectively. As shown in the negative impedance converter of Fig.1, both the Z and Y terminals are connected together, and this point also serves as the input of the complete negative impedance converter circuit with respect to ground. In literature, CCII is available in both positive and negative versions, which is defined by the sign of the current i_z in Fig. 1. In this paper, a positive current
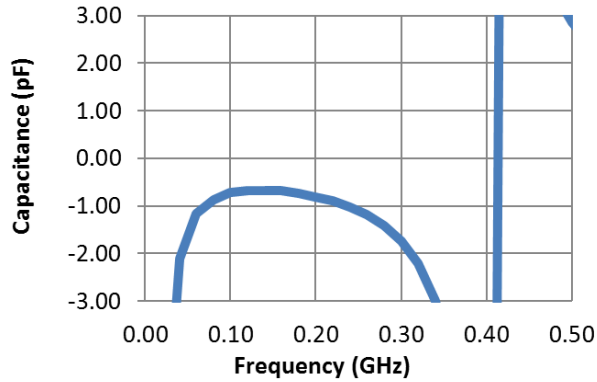

Fig. 3. Simulation results showing input capacitance observed at Z_{in} for a load capacitor Z_L of 1.3 pF for the circuit in Fig. 1 (computed capacitance values above the resonance near 400 MHz are anomalous due to zero crossing of Im(Z)).
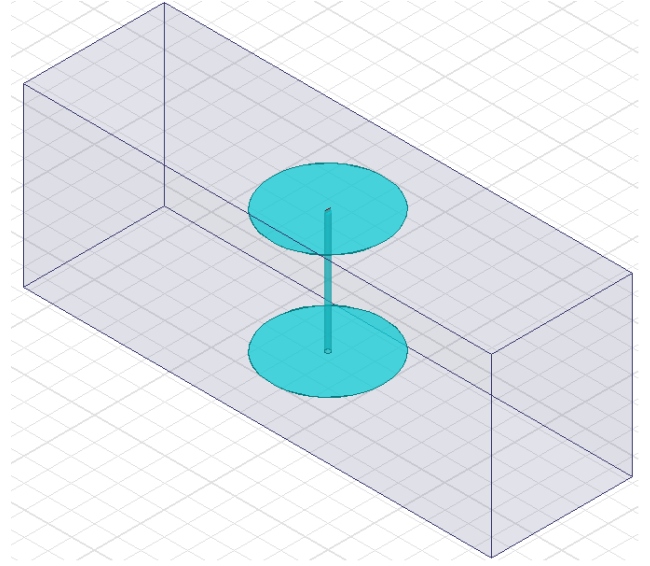

Fig. 4. Electric disk resonator (EDR) metamaterial sample used in simulation. The diameter of the disks is 48mm. The height of the center post is 105mm, and its radius is 2.25mm. The EDR is loaded via a gap in the post, located just under the upper disk. The EDR was simulated in a rectangular waveguide where the upper and lower plates were defined as PEC and positioned 150mm apart, and the side plates were defined as PMC and positioned 120mm apart.

conveyor (CCII+) device is used.

In Fig.1, Z_{IN} is the input impedance and Z_L is the load impedance of the circuit. The transistors M1 and M4 are the current sources set by Bias1 and Bias2.

From Fig. 1, the voltage on the node at terminal X is,

$$v_x = -i_x Z_L \ , \qquad (2)$$

and from (1) it can be noted that, $v_x = v_y$, and $i_z = i_x$, then equation (2) becomes

$$v_y = -i_z Z_L \ . \qquad (3)$$

At the input terminal, Y, the input voltage is $v_{in} = v_y$.

When KCL is applied at terminal Y, it yields $i_{in} = i_y + i_z$, but according to (1), $i_y = 0$. Therefore $i_{in} = i_z$, and (3) becomes

$$v_{in} = -i_{in} Z_L \ , \qquad (4)$$

and therefore the input impedance Z_{in} is

$$Z_{in} = \frac{v_{in}}{i_{in}} = -Z_L \ . \qquad (5)$$

III.   SIMULATION RESULTS

The circuit in Fig. 1 shows the basic schematic of the CMOS implementation of the negative impedance converter. Fig. 2 shows the simulation results for input impedance Z_{in} of the circuit in Fig. 1 when simulated with a 1.3 pF load Z_L, where the real part of Z_{in} is shown in solid blue and the imaginary part of Z_{in} shown in dotted red. In this all pMOS transistors are 100×0.5 microns and all nMOS transistors are 50×0.5 microns. As shown in Fig. 2, the dotted red imaginary part of the impedance curve follows an inverted positive capacitance profile, resulting in a negative capacitor.
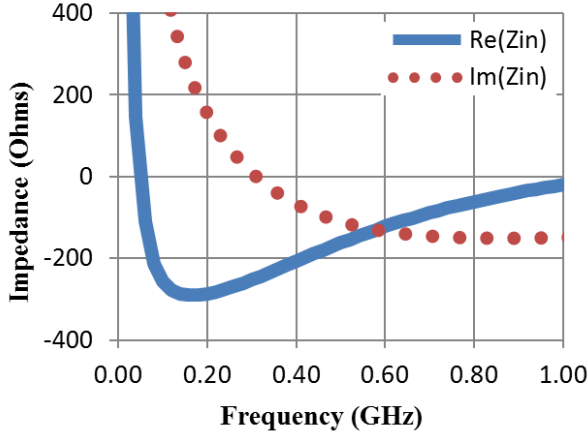
Fig. 5. Simulation results showing input impedance Z_{in} with real part (solid blue) and imaginary part (dotted red) for a 4 pF load capacitor Z_L for the circuit in Fig. 1

The resulting negative capacitance at the input of Fig. 1 is shown in Fig. 3, where the observed negative capacitance is -700 fF at low frequency. It must be noted that, this circuit works as a negative capacitor up to 400 MHz and any values after 400 MHz are anomalous due to zero crossing of the imaginary part of the input impedance in Fig. 2.

IV. EFFECTS ON METAMATERIALS

As noted earlier, one of the target applications for these negative capacitors is wideband metamaterials [17]. As shown above, the forgoing designs exhibit parasitic resistance in addition to the desired negative capacitance. Therefore, it is also useful to investigate the effect of such parasitic resistance on the overall metamaterial performance. Following the results above, the EDR (Electric Disk Resonator) metamaterial in Fig. 4 is evaluated with a negative capacitor load to observe the effects of undesired parasitic resistance [17].

The structure in Fig. 4 requires a -4 pF capacitance for the desired metamaterial behavior. Therefore, Fig. 5 shows the predicted impedance for the circuit of Fig. 1 with a load of 4 pF, where the real part of Z_{in} is shown in solid blue and the imaginary part of Z_{in} shown in dotted red. Note that, the
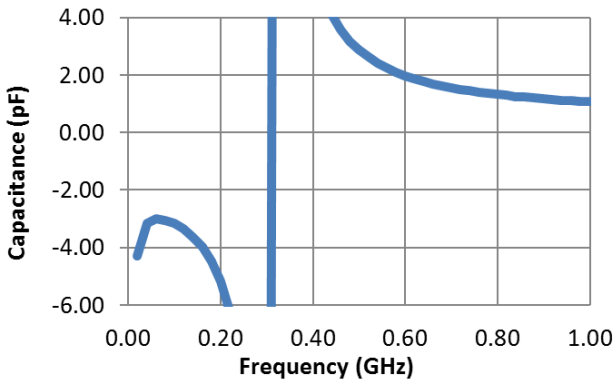

Fig. 6. Simulation results showing input capacitance observed at Z_{in} for a load capacitor Z_L of 4 pF for the circuit in Fig. 1 (computed capacitance values above the resonance near 300 MHz are anomalous due to zero crossing of Im(Z)).
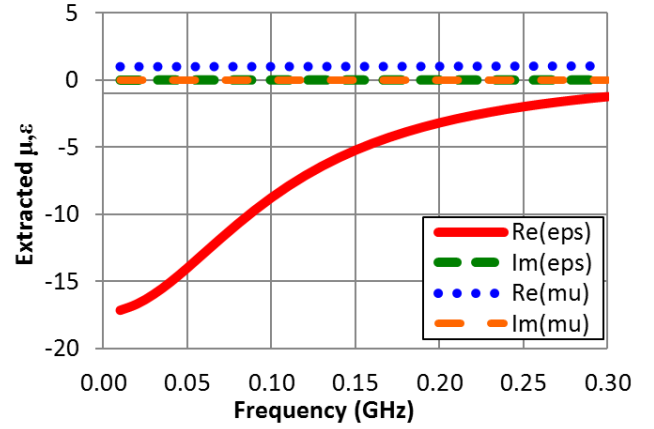

Fig. 7. Extracted values for Re{μ}, Im{ μ}, Re{ε}, and Im{ε} in the ideal case, over the frequency range 10 MHz-300 MHz .

imaginary part of the impedance curve in Fig. 5 follows an inverted positive capacitance profile, indicating negative capacitance. The resulting negative capacitance value at the input of Fig. 1 for a load of 4 pF is shown in Fig. 6, where the observed negative capacitance is approximately -4 pF.

As illustrated in Figs. 5 and 6, the capacitor has a value of approximately -4 pF, and an associated series resistance of approximately -290 Ω over the range from 50 MHz to 200 MHz. This can affect the application to metamaterial structures like that shown in Fig. 4. Therefore, the response of this metamaterial was simulated in HFSS for both the ideal capacitor with a nominal value of -4 pF and no series resistance, and for the non-ideal capacitor with a nominal value of -4 pF and a series resistance of -290 Ω.

The EDR was simulated first for the ideal case, with no series resistance. Fig. 7 shows the extracted values for Re{μ}, Im{μ}, Re{ε}, and Im{ε}, over the frequency range 10 MHz to 300 MHz [18]. The EDR was next simulated for the non-ideal case, including -290 Ω of series resistance. Fig. 8 shows the extracted values for Re{μ}, Im{μ}, Re{ε}, and Im{ε} for this case. Thus, it can be seen that the series resistance adversely
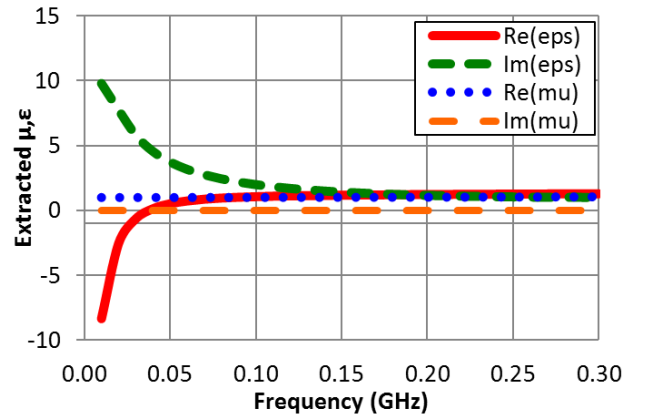
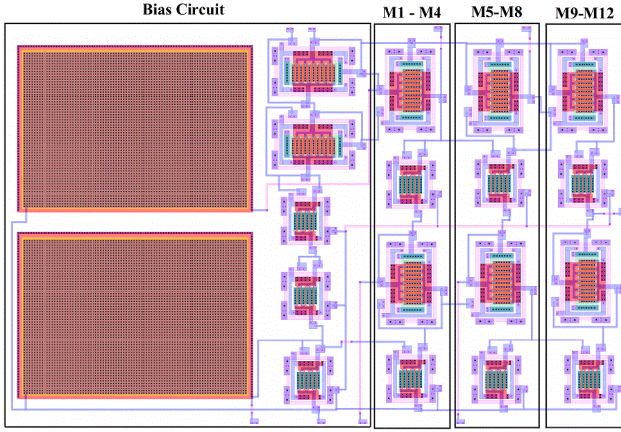Fig. 8. Extracted values for Re{μ}, Im{ μ}, Re{ε}, and Im{ε} in the non-ideal case, over the frequency range 10 MHz-300 MHz.

Fig. 9. Detailed layout of second generation current conveyor (CCII+) circuit in 0.5 micron CMOS design process.

Fig. 11. Measured results showing input impedance Z_{in} with real part (solid blue) and imaginary part (dotted red) for a 1.3 pF load capacitor Z_L for the circuit in Fig. 1.

affected the performance of the metamaterial. Nevertheless, negative permittivity is still observed over parts of the frequency spectrum.

In the case including -290 Ω, it can be observed that Re{ε} ≈ Im{ε} over a large portion of the spectrum, suggesting a gain medium with associated propagation constant [19].

$$\gamma = \alpha + \mathrm{j}\beta = j\omega\sqrt{\mu(\varepsilon' - j\varepsilon'')} = j\omega\sqrt{\mu\varepsilon'e^{-j\pi/4}} \quad . \quad (6)$$

V. MEASURED RESULTS

The layout of the current conveyor in Fig. 1 is presented in Fig. 9, which has been fabricated in a 0.5 micron CMOS process. For this design, all pMOS transistors are 100×0.5 microns and all nMOS transistors are 50×0.5 microns. The fabricated circuit was measured using a vector network analyzer from 10 MHz to 500 MHz and the measured results are shown in Fig. 11 and Fig. 12 respectively. The measured results show a negative capacitance of –0.65 pF for an on-chip load of 1.3 pF.

VI. CONCLUSION

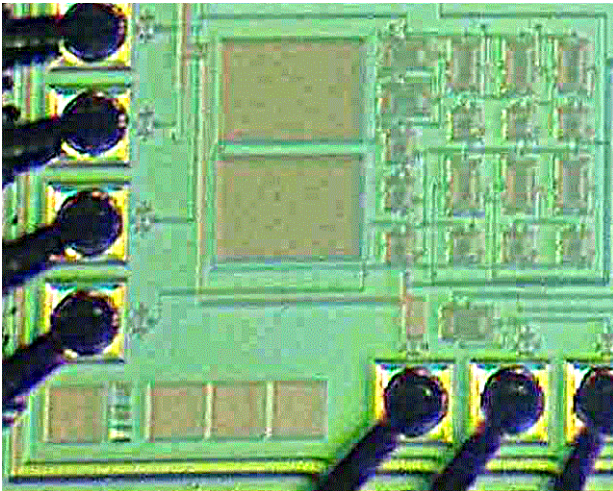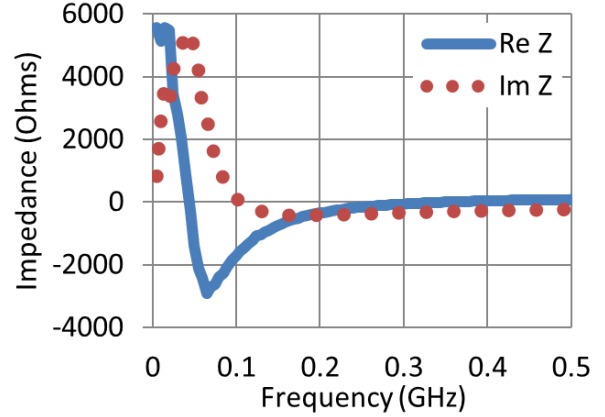A simple second generation negative impedance convertor

is implemented using a current conveyor circuit, which has been analyzed, simulated and measured in a 0.5 micron CMOS process. The measured negative capacitor values compared favorably with what was expected from the analysis and simulation, despite the fact that a negative parasitic resistance is observed on the input as expected. The effect of this parasitic negative resistance in addition to the desired negative capacitance on the overall wideband metamaterial structure (Electric Disk Resonator) was also studied and the simulation results were presented. It was found that while negative permittivity could still be achieved in the presence of parasitic negative resistance, there was an adverse effect on the bandwidth and performance of the overall structure.

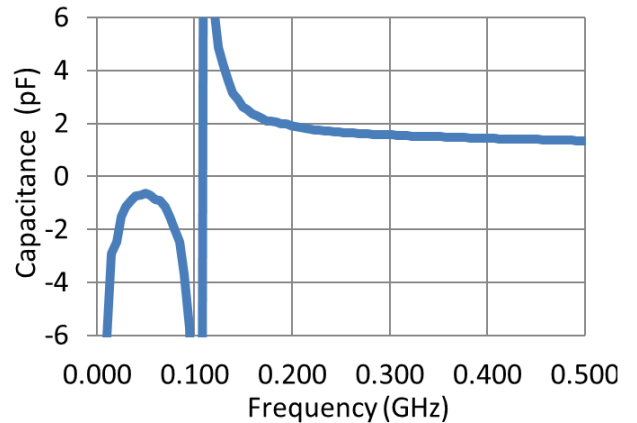Fig. 10. Current conveyor circuit on-chip fabricated in a 0.5 micron CMOS process.

Fig. 12. Measured results showing input capacitance observed at Z_{in} for a load capacitor Z_L of 1.3 pF for the circuit in Fig. 1.

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