Compensation of Frequency Dependent Parasitic Resistance in a CMOS Linvill Negative Inductor

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***Abstract*— This paper presents an effective approach for reducing parasitic resistance of a CMOS negative inductor with a single compensating resistor. A compensating resistor is used to mitigate the effect of parasitic resistance with quadratic frequency dependence. The undesired parasitic effect is induced by the inevitable finite drain-source resistance of the input CMOS transistor of the most common Linvill negative inductor configuration. In particular, a two-transistor Linvill negative impedance inverter is considered. Theoretical analysis and circuit simulations show that the parasitic CMOS drain-source resistance leads to this undesired quadratic frequency dependency, and the proposed simple compensation circuit is effective. Measured results are given for a prototype CMOS circuit demonstrating the proposed compensation method.**

***Keywords*— negative inductance; quadratic frequency dependence; negative impedance inverter; CMOS; integrated circuit; non-Foster circuit**

I. Introduction

Non-Foster circuits such as negative inductors and negative capacitors offer the potential for increased bandwidth in a variety of applications such as wideband antennas, artificial magnetic conductors, and metamaterials with negative permeability [1]. For antennas, negative inductors can be used to achieve miniaturized, compact, multi-frequency or multi-function characteristics [2]. More recently, negative inductors have been used to create wideband artificial magnetic conductors to mitigate natural resonances of the inherently narrowband periodic grid of metallic patches that comprise these devices [3], [4]. Also, in metamaterials, negative inductors enable wideband negative permeability while eliminating the inherent narrowband resonances of a classical split-ring resonator [5], [6]. In all these applications it will be advantageous to use CMOS processes. Therefore, an improved CMOS negative inductor design is considered in this paper.

In particular, a two transistor CMOS negative inductor design is considered. This design is based on a Linvill negative impedance inverter circuit [7]. Although bipolar implementations of these circuits are common, it is easy to achieve broad compatibility with common system-on-a-chip processes using a CMOS implementation. CMOS implementations are less common due to performance limitations induced by CMOS transistor characteristics [8], [9]. In particular, a parasitic resistance with quadratic frequency dependence is commonly seen in this CMOS negative inductor circuit. Therefore, a simple and effective compensation technique is proposed in this paper that does not require oversized transistors or wasteful bias current.

In the following sections the theory and limitations of the basic CMOS Linvill design is first considered, including the expected parasitic impedance resulting due to the CMOS transistors. In addition the theory of the compensation circuit is introduced. In the subsequent section, simulations show reduced parasitic resistance, improved Q, and compensation of quadratic frequency dependency using the proposed compensation method. Finally the layout and measured results of the proposed negative inductance circuit fabricated in 0.5μm CMOS process is presented.

II. Basic Proposed Circuit Design and Analysis

The block diagram of Linvill negative inductance circuit is shown in Fig. 1. In this circuit, the input port impedance Z_{in} is a function of the load impedance Z_L, as in prior bipolar transistor implementations, where $Z_{in}=-K/Z_L$ [10]. The detailed schematic including bias circuit used for this design is shown in Fig. 2, where the transistors M1 and M2 are the primary Linvill transistors, and resistors R_1 and R_2 establish a scaling factor for the inversion of the load impedance Z_L. Also, the bias current is by transistor M3 mirrored through transistor M4.

To analyze the circuit in Fig. 2, consider a small signal analysis of the circuit shown in Fig. 3 that includes parasitic impedances Z_{ds1}, Z_{gs1}, Z_{gd1}, Z_{ds2}, Z_{gs2} and Z_{gd2}. The Input impedance Z_{in} is given by, V_i / i_i , and Z_{in}, is found by solving the following three nodal equations at nodes V_i, V_2 and V_L in Fig. 3:

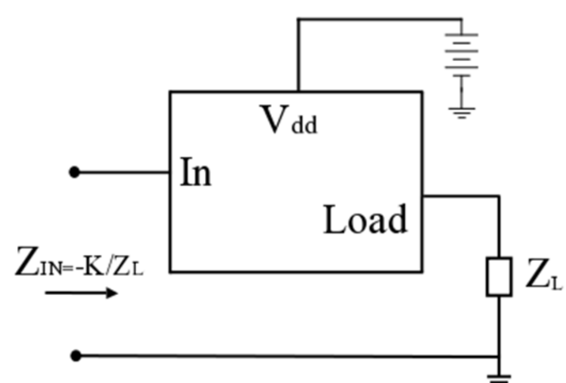

Fig. 1. Block diagram of the proposed negative inductor circuit.

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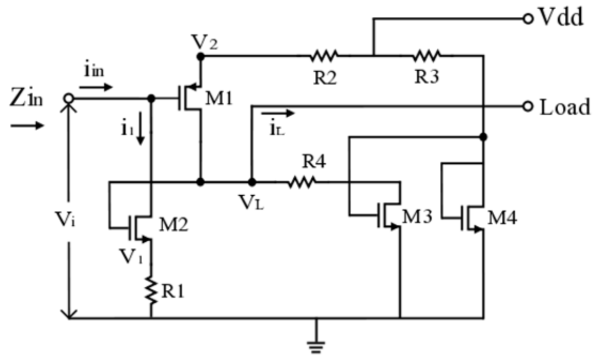

Fig. 2 Schematic of proposed negative inductance circuit, including bias circuit detail.

$$\left(-g_1 - \frac{1}{Z_{gs1}}\right)V_i + \left(-\frac{1}{Z_{ds1}}\right)V_L + \left(g_1 + \frac{1}{Z_{ds1}} + \frac{1}{Z_{gs1}} + \frac{1}{R_2}\right)V_2 = 0 \qquad (1)$$

$$\left(g_1 - \frac{1}{Z_{gd1} \| Z_{gd2}}\right)V_i + \left(\frac{1}{Z_{ds1}} + \frac{1}{Z_{gd1} \| Z_{gd2}} + \frac{1}{Z_L \| Z_{gs2}}\right)V_L + \left(-g_1 - \frac{1}{Z_{ds1}}\right)V_2 = 0 \qquad (2)$$

$$\left(\frac{1}{Z_{ds2}} + \frac{1}{Z_{gs1}} + \frac{1}{Z_{gd1} \| Z_{gd2}}\right)V_i + \left(g_2 - \frac{1}{Z_{gd1} \| Z_{gd2}}\right)V_L + \left(-\frac{1}{Z_{gs1}}\right)V_2 - 1 = 0, \qquad (3)$$

where g_1 and g_2 are the trans-conductance of transistors M1 and M2, where Z_{ds1}, Z_{gs1} and Z_{gd1} are the drain-source, source-gate, and gate-drain parasitics of M1, where Z_{ds2}, Z_{gs2} and Z_{gd2} are the respective drain-source, source-gate, and gate-drain impedances of transistor M2.

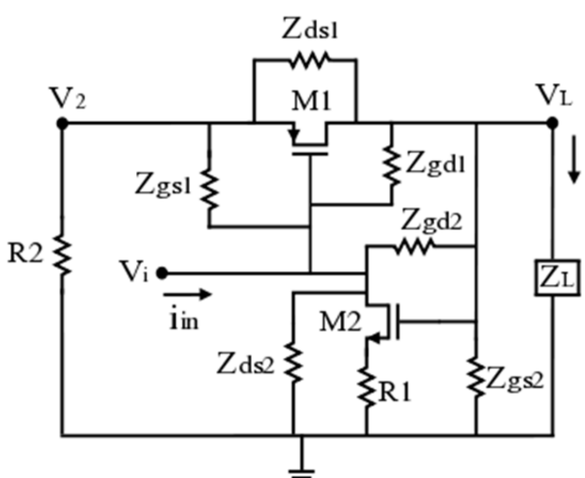

Fig. 3. Schematic of the proposed negative inductor circuit for analysis purposes that includes parasitic impedances.

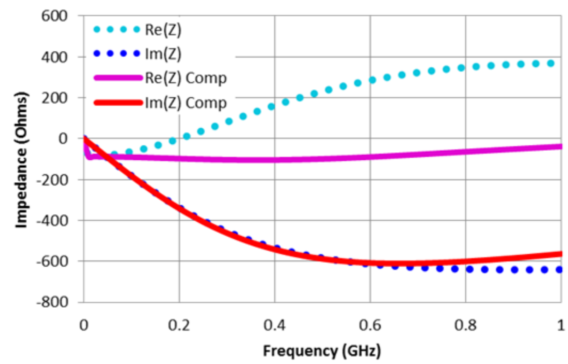

Fig. 4. Theoretically calculated results in Mathcad showing compensated and uncompensated input impedance results. The solid lines are the compensated circuit with Re(Z) as the upper solid magenta curve and with Im(Z) as the lower solid red curve. The dotted lines are for the uncompensated circuit with Re(Z) as the upper dotted cyan curve and with Im(Z) as the lower dotted blue curve.

When these three nodal equations were solved for Z_{in} using Mathcad, the solution is a large equation with many variables, too large to include here. Nevertheless, this solution for Z_{in} is plotted in Mathcad between 10 MHz to 2 GHz in Fig. 4 with dotted lines for the uncompensated circuit with Re(Z) as the upper dotted cyan curve and with Im(Z) as the lower dotted blue curve. The solid lines in Fig. 4 are the compensated circuit (described later) with Re(Z) as the upper solid magenta curve and with Im(Z) as the lower solid red curve. In addition, it was observed that the stray impedances C_{gd1}, C_{gd2}, R_{ds2} and C_{ds2} tended to have larger influence on the input impedance Z_{in}.

The circuit was also simulated in Agilent ADS. In the proposed design, all nMOS transistors are 50×0.5 µm and all pMOS transistors are 100×0.5 µm. From the simulation, nMOS transistor M2 has transconductance $g_2 = 0.0055$ S, and pMOS transistor M1 has a transconductance of $g_1 = 0.00314$ S. Also, the values of stray impedances and capacitances are R_p=3244 Ω, R_2=1000 Ω, R_3=3000 Ω, $C_{gs1}=1.04\times10^{-13}$ F, $C_{gd1}=3\times10^{-14}$ F, R_{ds1}=6850 Ω, $C_{ds1}=4.2\times10^{-14}$ F, $C_{gs2}=4.556\times10^{-14}$ F, $C_{gd2}=1.1\times10^{-14}$ F, R_{ds2}=3077 Ω, and $C_{ds2}=2.4\times10^{-14}$ F. It can be seen that the theoretical calculations in Fig. 4 closely match the ADS results of Fig. 5. In Fig. 5, the dashed lines show the uncompensated circuit with Re(Z) as the upper dashed cyan curve and with Im(Z) as the lower dashed blue curve. The solid lines in Fig. 5 show the compensated circuit (described later) with Re(Z) as the upper solid magenta curve and with Im(Z) as the lower solid red curve.

It was observed that the parasitic resistance R_{ds2} of M2 in Fig. 3 greatly influence the input impedance Z_{in}. As noted earlier, there is a parasitic resistance with quadratic frequency dependence of the real part of Z_{in}. To see how this parasitic resistance arises, reconsider Fig. 3 with only $Z_{ds2}=R_{ds2}$, and $Z_{gs1}=Z_{ds1}=Z_{gd1}=Z_{gd2}=Z_{gs2}=\infty$. Then, the input current, i_i is approximated as

$$i_i \approx i_1 = g_2(v_L - v_1) + \frac{(v_i - v_1)}{R_{ds2}}, \qquad (4)$$

where i_1 is the drain current of transistor M2, and g_2 is the transconductance of transistor M2, R_{ds2} is the drain source

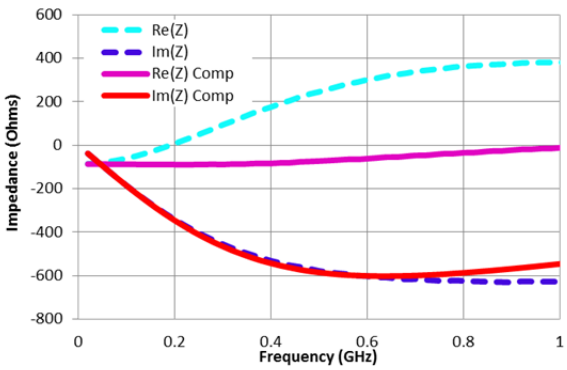

Fig. 5. ADS simulation results. The dashed lines show the uncompensated circuit with Re(Z) as the upper dashed cyan curve and with Im(Z) as the lower dashed blue curve. The solid lines show the compensated circuit with Re(Z) as the upper solid magenta curve and with Im(Z) as the lower solid red curve.

resistance of transistor M2. Since $v_1 = i_1 R_1 \approx i_i R_1$, substituting for v_1 in (4) and rearranging yields

$$i_i(R_{ds2} + g_2 R_1 R_{ds2} + R_1) - v_i = g_2 v_L R_{ds2}. \qquad (5)$$

For the case $R_1 = 0$,

$$i_i R_{ds2} - v_i = g_2 v_L R_{ds2}\,. \qquad (6)$$

To solve for v_L in terms of v_i, let $v_L = i_L Z_L$ and $i_L = -i_2$, so $v_L = -i_2 Z_L$. Since $i_2 = g_1 (v_i - v_2)$,

$$v_L = -i_2 Z_L = -g_1(v_i - v_2)Z_L\,. \qquad (7)$$

where Z_L is the load impedance in Fig. 3. Since $i_L = -i_2$, then $v_L/Z_L = -v_2/R_2$, and $v_2 = -v_L R_2/Z_L$. Substituting this result for v_2 in (7) gives

$$v_L = -g_1 Z_L v_i/(1 + g_1 R_2)\,. \qquad (8)$$

Finally, combining (6) and (8) results in

$$Z_{in} = \frac{v_i}{i_i} \approx \frac{(1+g_1R_2)R_{ds2}}{1+g_1R_2-g_1g_2R_{ds2}Z_L}, \qquad (9)$$

where Z_{in} is the desired expression for the approximation of input impedance of the circuit in Fig. 3. The load Z_L in (9) is a capacitor C with a parallel resistance R_p due to transistors M1, M2 and M3, so the load impedance is given as

$$Z_L = C||R_p, \qquad (10)$$

where $R_p = (R_{ds1} + R_2)||\,(R_3 + R_{ds3})$.

To see the dominant mechanism in creating the undesired parasitic resistance with quadratic frequency dependence, the result in (9) can be approximated (after much rearrangement) as

$$Z_{in} \approx \frac{-j\omega K_1}{K_3} + \omega^2 \frac{R_{ds2}{K_2}^2}{{K_3}^2}, \qquad (11)$$

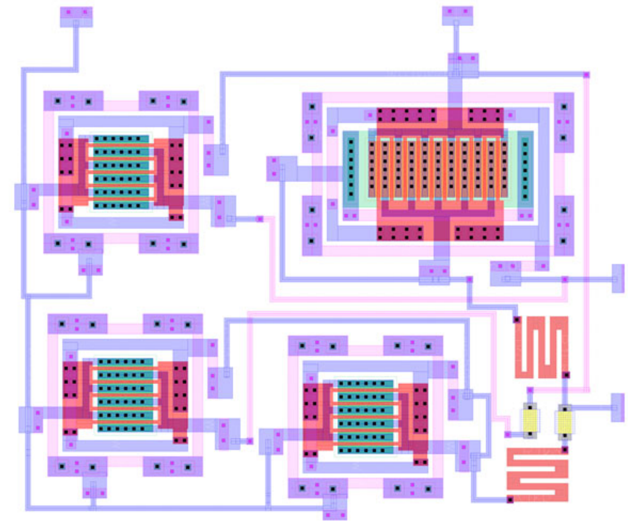

Fig. 6. Layout of Negative Inductance Circuit with bias shown.

where $K_1 = R_{ds2}\,(1+g_1R_2)$, $K_2 = 1+\, g_1R_2$, and $K_3 = R_{ds2}\,(g_1g_2)/C$. The above result in (11) shows that the input impedance Z_{in} is a negative inductance $L = -K_1/K_3$ in series with a resistance having a quadratic frequency dependence due to ω^2 term. In addition R_{ds2} plays a dominant role in this parasitic resistance since the quadratic term disappears when $R_{ds2}=0$. Furthermore, this quadratic frequency dependence of Re(Z) can be seen in the plots of Figs. 4 and 5.

III. Compensation Method

It was found that a compensating resistor R_s can be applied in series with the load capacitance C to reduce the quadratic frequency dependence. To see this, consider the circuit in Fig. 1 where Z_L is a resistance R_s added in series with the conventional load capacitance C. This results in:

$$Z_{in} = \frac{-K}{Z_L} = \frac{-K}{Rs + \frac{1}{j\omega C}} = \frac{1}{-\frac{R_S}{K} - \frac{1}{j\omega KC}} = -\frac{K}{R_s}|| - j\omega KC, \qquad (12)$$

where a series resistance $-K/R_s$ appears in parallel at the input Z_{in}. This new parallel negative input resistance can be used to cancel the undesired effects of $Z_{ds2}=R_{ds2}$ in (11), since R_{ds2} also appears in parallel with the input Z_{in}. When $K/R_s=R_{ds2}$, then R_{ds2} in parallel with K/R_s becomes an open circuit, and the input impedance Z_{in} becomes a pure reactance, and the quadratic term in (11) disappears.

The Re(Z) for the compensating circuit is shown as the upper solid magenta curves Fig. 4 and Fig. 5. In these results the compensating resistor R_s is 275 ohms, and the load capacitance C is 1 pF. In Fig. 4 and 5, the quadratic frequency dependence of Re(Z) is greatly reduced, and there is almost no change of Re(Z) over frequency from dc to 400 MHz. In the compensated and uncompensated cases of Fig. 4 and 5, Im(Z) is seen to be the desired negative inductance as evidenced by the downward slope of Im(Z) from dc to approximately 600 MHz. Beyond 600 MHz, the Im(*Z*) is dominated by a parasitic capacitance of 0.13 pF. At low frequencies, the input

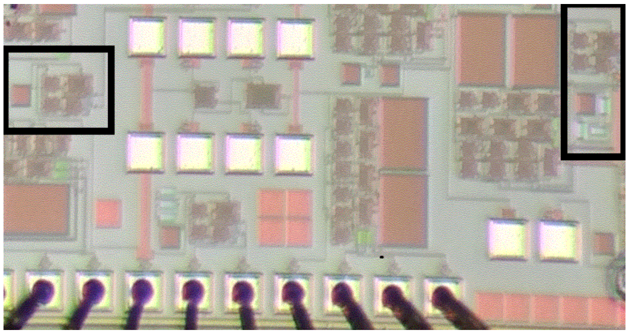

Fig. 7. Photograph of negative inductance circuit, where the black box on the left encloses the uncompensated design and the black box on the right encloses the compensated design.

impedance is approximately -87 ohms resistance in series with a -300 nH inductance.

IV. Measured Results

The layout of the proposed design in 0.5 micron CMOS is shown in Fig. 6. A photograph of the chip is shown in Fig. 7, where the black box on the left encloses the uncompensated design and the black box on the right encloses the compensated design. Vdd was adjusted to 4.1 V and 1.5 V dc bias at V_i to compensate for actual resistance values on the fabricated chip and approximately the original current levels. Measured results are shown in Fig. 8, where the dashed lines are for the uncompensated circuit with Re(Z) as the upper dashed cyan curve and with Im(Z) as the lower dashed blue curve. The solid lines in Fig. 8 are the compensated circuit with Re(Z) as the upper solid magenta curve and with Im(Z) as the lower solid red curve. As can be seen, the compensation circuit reduces the frequency dependence of Re(Z) in the measured results of Fig. 8. The measured results in Fig. 8 correspond well with the simulated results in Fig 5 up to about 200 MHz. More importantly the compensation method reduces parasitic resistance effects both in the measured results of Fig. 8 and simulated results in Fig. 5.

V. Conclusion

A Linvill negative inductor circuit is presented and designed in 0.5 micron CMOS process. The transistors introduce a frequency dependent parasitic resistance at the input impedance that is accounted for in the analysis. The proposed circuit incorporates a single compensating resistor Rc placed in series with the load capacitor, such that it greatly mitigates the frequency dependency of the parasitic resistance. This compensation method is a simple and effective approach for decreasing quadratic frequency dependent parasitic resistance in CMOS transistor circuit without the complexity of oversized transistors or wasteful bias current. Simulation and measured results confirm the efficacy of the approach.

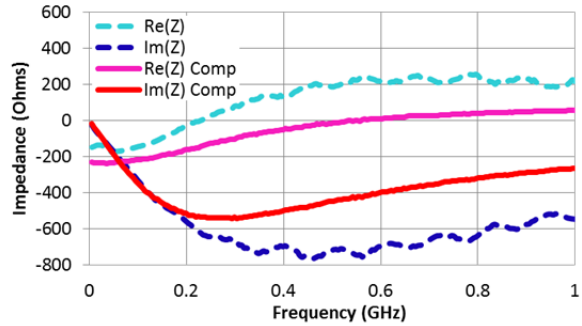

Fig. 8. Measured results showing compensated and un-compensated input impedance results. The solid lines are the compensated circuit with Re(Z) as the upper solid magenta curve and with Im(Z) as the lower solid red curve. The dashed lines are for the uncompensated circuit with Re(Z) as the upper dashed cyan curve and with Im(Z) as the lower dotted blue curve.

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