

# A DC-Coupled Negative Inductance Circuit with Integrated Bias

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**Abstract**—Negative inductance circuits offer the potential for increased bandwidth in a variety of applications such as artificial magnetic conductors and metamaterials with negative permeability. To address such applications, a CMOS dc-coupled negative inductance circuit with integrated bias circuits is presented. The dc-coupled input is tailored to operate at low voltages and accommodate applications having an inductive load in series with a low resistance. An integrated bias circuit is used to allow operation with a single power supply and to eliminate the need for a separate input bias. In addition, the parasitic capacitance of the CMOS transistors in the basic negative impedance inverter is used to set the negative inductance of the overall circuit. Results are presented that show a negative inductance of -110 nH in a 0.5 micron CMOS process.

**Keywords**—negative inductance; negative impedance inverter; CMOS; integrated circuit

## I. INTRODUCTION

The potential for increased bandwidth has motivated the investigation of negative inductance circuits for a number of new applications. In artificial magnetic conductors, negative inductors are used to mitigate natural resonances of the inherently narrowband periodic grid of metallic patches that comprise these devices [1], [2]. In metamaterials, negative inductors are used in place of capacitors to eliminate the inherent narrowband resonances of a classical split-ring resonator while enabling broadband negative permeability [3]-[5]. In such applications, the negative inductor results in a non-Foster circuit that is not constrained by the Foster reactance theorem [6].

To serve such applications, a dc-coupled CMOS negative inductance with integrated bias circuits is proposed. Although negative inductance circuits commonly employ bipolar transistors, a CMOS implementation provides broad compatibility with common system-on-a-chip processes. A modified Linvill circuit is chosen, using a 0.5 micron CMOS process [7]-[9]. The proposed dc-coupled negative inductance circuit is designed to cancel or neutralize an external grounded positive inductive load in series with a low resistance. This dc coupling provides circuit bias without need for an additional external bias power supply. The proposed CMOS negative inductor design consists of a Negative Impedance Inverter (NII) comprised of a pair of cross-coupled CMOS transistors

that inverts the impedance of a load reactance. In addition, the circuit uses the parasitic capacitance of the transistors as the load capacitance that is converted to a negative inductance.

In the next section, the analysis of the basic negative inductance circuit is first presented, including the expected parasitic capacitance resulting due to the CMOS transistors. The subsequent section describes the detailed design and layout of the proposed circuit, and the final section provides simulation results that demonstrate performance of the proposed negative inductance circuit with integrated bias.

## II. PROPOSED CIRCUIT AND ANALYSIS

The negative inductance circuit is shown in Fig. 1 and is a CMOS implementation based on a form of Linvill negative impedance inverter [7], [8]. In this circuit, the input port impedance  $Z_{in}$  is a function of the load impedance  $Z_L$ , as in prior bipolar transistor implementations. In the topology shown, transistors M1 and M2 provide feedback to the input  $Z_{in}$ , where resistors  $R_1$  and  $R_2$  establish a scaling factor for the inversion of the load impedance  $Z_L$ .

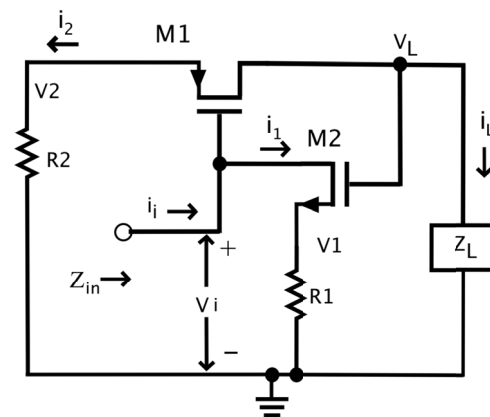


Fig. 1. Basic Negative Impedance Inverter (NII) circuit for analysis purposes.

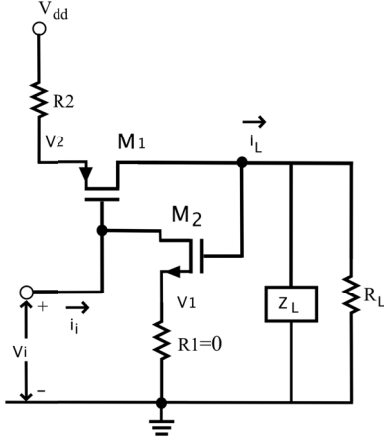


Fig. 2. Schematic of the proposed negative inductor circuit for analysis purposes.

To find the input impedance  $Z_{in}$  for the circuit in Fig. 1, first consider input current  $i_i$ :

$$i_i \approx i_1 = g_2(v_L - v_1), \quad (1)$$

where  $i_1$  is the drain current of transistor M2, and  $g_2$  is the transconductance of transistor M2. Since  $v_1 = i_1 R_1 \approx i_i R_1$ , substituting for  $v_1$  in (1) and rearranging yields

$$i_i(1 + g_2 R_1) = g_2 v_L. \quad (2)$$

Next, solve for  $v_L$  in terms of  $v_i$ . To begin,  $v_L = i_L Z_L$  and  $i_L = -i_2$ , so  $v_L = -i_2 Z_L$ . Since  $i_2 = g_1(v_i - v_2)$ ,

$$v_L = -i_2 Z_L = -g_1(v_i - v_2) Z_L. \quad (3)$$

where  $Z_L$  is the load impedance in Fig. 1. Since  $i_L = -i_2$ , then  $v_L/Z_L = -v_2/R_2$ , and  $v_2 = -v_L R_2/Z_L$ . Substituting this result for  $v_2$  in (3) then gives

$$v_L = -g_1(v_i + v_L R_2/Z_L) Z_L. \quad (4)$$

Rearranging to solve for  $v_L$  gives

$$v_L = -\frac{g_1 Z_L}{1 + g_1 R_2} v_i. \quad (5)$$

Finally, combining (2) and (5) results in,

$$Z_{in} = \frac{v_i}{i_i} = \frac{(1 + g_2 R_1)(1 + g_1 R_2)}{g_1 g_2} \left( \frac{-1}{Z_L} \right), \quad (6)$$

where  $Z_{in}$  is the desired expression for the input impedance of the circuit in Fig. 1. From (6), the circuit is seen to be a negative impedance inverter, since  $Z_{in}$  is proportional to  $-1/Z_L$ .

The result in (6) can be approximated for the case where  $g_2 R_1 \gg 1$  and  $g_1 R_2 \gg 1$ , where (6) becomes

$$Z_{in} \approx R_1 R_2 \left( \frac{-1}{Z_L} \right). \quad (7)$$

Next, the proposed circuit is shown in Fig. 2, and corresponds to the circuit of Fig. 1, but with  $R_1 = 0$ , and so differs from more common implementations of negative inductance. In addition, an inherent loading resistor  $R_L$  is shown in Fig. 1, since it is part of the proposed biasing scheme.

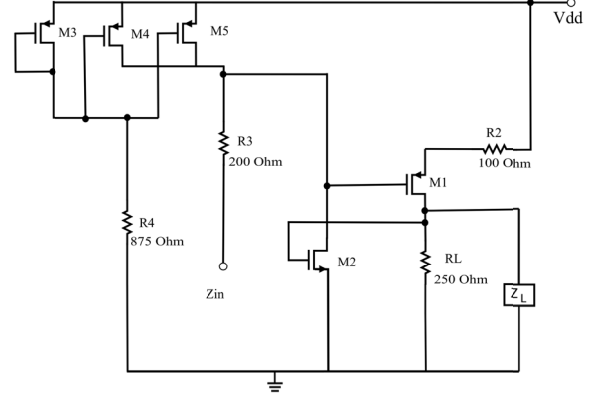


Fig. 3 Schematic of proposed negative inductance circuit, including bias circuit detail.  $R_L$  in circuit above corresponds to  $R_L$  in (11), and  $R_2$  above corresponds to  $R_2$  in (11).

Furthermore, the proposed circuit uses the parasitic capacitance of the transistors as the capacitive load  $Z_L$ .

The analysis of the proposed circuit in Fig. 2 follows along similar lines to Fig. 1, but with important differences. To begin, the input current from (2) becomes

$$i_i = g_2 v_L, \quad (8)$$

since resistor  $R_1$  has changed, with  $R_1 = 0$ .

In addition, the load impedance  $Z_L$  now has a parallel resistor  $R_L$  that is part of the bias circuit. So, let the new load impedance be  $Z'_L = Z_L || R_L$ . Then, the load voltage  $v_L$  in (5) becomes

$$v_L = -\frac{g_1 Z'_L}{1 + g_1 R_2} v_i. \quad (9)$$

Combining equations (8) and (9) and rearranging gives the new input impedance  $Z'_{in}$  for the proposed circuit of Fig. 2.

$$Z'_{in} = \frac{v_i}{i_i} = \frac{(1 + g_1 R_2)}{g_1 g_2} \left( \frac{-1}{Z'_L} \right), \quad (10)$$

From (10), the circuit of Fig. 2 is also seen to be a negative impedance inverter, with input impedance  $Z'_{in}$  proportional to  $-1/Z'_L$ . Since  $R_L$  and  $Z_L$  comprising  $Z'_L$  are in parallel, the input impedance can also be written as

$$Z'_{in} = \frac{v_i}{i_i} = \frac{(1 + g_1 R_2)}{g_1 g_2} \left( \frac{-1}{Z_L} + \frac{-1}{R_L} \right). \quad (11)$$

The final proposed circuit including bias circuit details is shown in Fig. 3.

### III. SIMULATION RESULTS

The proposed negative inductance circuit of Fig. 3 was designed in 0.5 micron CMOS and simulated in Agilent ADS. In the design, all nMOS transistors had width×length of 50×0.5  $\mu\text{m}$  and all pMOS transistors were 100×0.5  $\mu\text{m}$ . This circuit uses the design values of  $R_L = 250$  ohms and  $R_2 = 100$  ohms for (11).

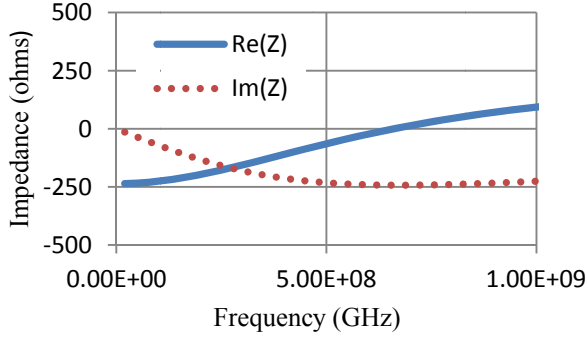


Fig. 4. Simulation results showing real part of input impedance  $Z_{in}$  (solid blue line) and imaginary part of  $Z_{in}$  (dotted red line) for  $R_L = 250 \Omega$ .

The simulation results of Fig. 4 show the real and imaginary parts of the input impedance  $Z_{in}$  for the proposed circuit of Fig. 3. Here, the negative inductance is evident in the downward trajectory of the imaginary part of  $Z_{in}$  (dotted red curve) at low frequencies below 500 MHz. This downward linear slope of the reactance of the negative inductor is the opposite of the case for a positive inductor. In addition, the expected parasitic negative resistance component from (11) is also seen in the plot of the real part of the input impedance (solid blue curve).

In simulation, nMOS transistor M2 has transconductance  $g_2 = 0.0036$  S with width $\times$ length of  $50 \times 0.5 \mu\text{m}$ , and pMOS transistor M1 has a transconductance of  $g_1 = 0.0053$  S with width $\times$ length of  $100 \times 0.5 \mu\text{m}$ . From (11), the predicted input impedance is then

$$Z'_{in} = \frac{v_i}{i_i} = 80,188 \left( \frac{-1}{Z_L} + \frac{-1}{R_L} \right), \quad (12)$$

with  $Z_L = 1/(j\omega C)$ , and where  $C$  is the load capacitance due to the parasitic capacitance of the two transistors. For the present case,  $C$  is approximately  $0.38$  pF, so (12) finally becomes

$$Z'_{in} = -320.8 - j\omega \cdot 30.5 \times 10^{-9}. \quad (13)$$

From the form of (13), the input impedance is a  $-320.8$

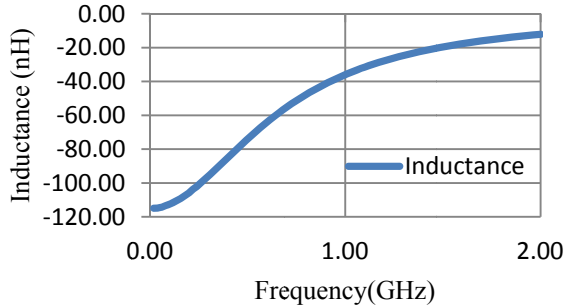


Fig. 5. Simulation results showing input inductance observed at  $Z'_{in}$  for  $R_L = 250 \Omega$ .

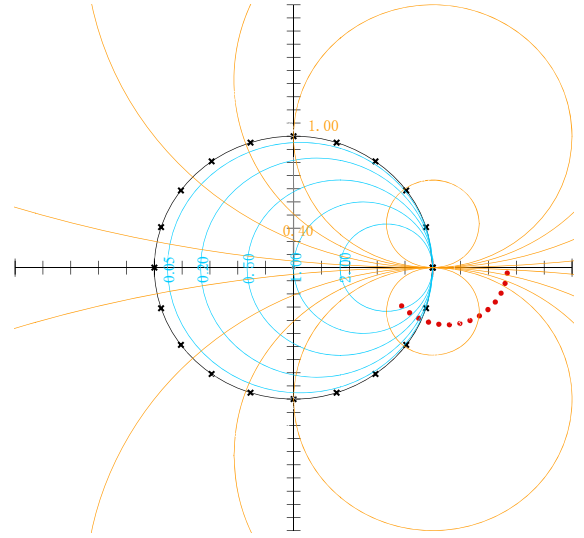


Fig. 6. Smith chart showing measured  $S_{11}$  of input impedance  $Z_{in}$ .

ohms resistance in series with a  $-30.5$  nH inductance. From Fig. 4, the observed negative resistance is  $-235$  ohms including a series internal positive resistance of  $R_3 = 200$  ohms in Fig. 3, thus implying an internal resistance of  $-435$  ohms seen at the gate of M1. From Fig. 5, the observed  $-115$  nH inductance is larger than predicted. Although it is suspected that the bias circuits may contribute to the difference, the present design was chosen because of its simplicity and the advantages of having the bias circuit integrated along with the remainder of the negative inductance circuit.

Fig. 6 shows a Smith chart for  $S_{11}$  (red dotted line) corresponding to  $Z_{in}$  for the circuit of Fig. 3. The plot of  $S_{11}$  is observed outside of the usual Smith chart region due to the negative resistance component of  $Z_{in}$  as predicted in (13) and seen in Fig. 4. Finally, the layout of the proposed design in  $0.5$  micron CMOS is shown in Fig. 7, where the overall size of the layout is  $230 \times 230$  microns. The design is currently scheduled for fabrication.

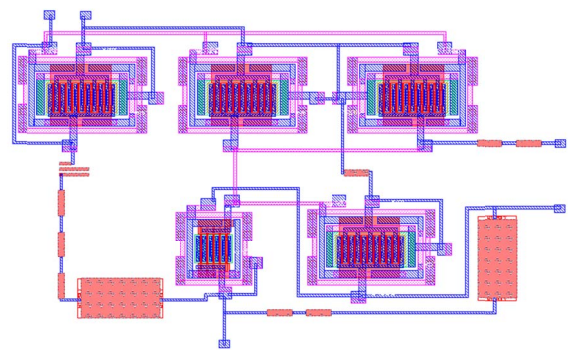


Fig. 7. Layout of Negative Inductance Circuit with bias shown.

#### IV. CONCLUSION

A negative inductor circuit is designed and analyzed. The circuit incorporates bias circuits, employs transistor parasitic capacitance as a load, and sets resistor  $R_l = 0$ . The bias arrangement also introduces a load resistance in parallel with the capacitive load that is accounted for in the analysis. The theoretical analysis of the circuit predicts a parasitic negative resistance in series with the desired negative inductance. Results are in fair agreement with the negative resistance component, while larger than expected negative inductance may be caused by surrounding bias circuits. Despite the increased inductance, the circuit offers useful negative inductance with the advantage of an integrated bias circuit.

#### ACKNOWLEDGMENT

This material is based upon work supported by the National Science Foundation under Grant No. ECCS-1101939.

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