NeuralWISP: A Wirelessly Powered Neural Interface With 1-m Range

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***Abstract*—We present the NeuralWISP, a wireless neural interface operating from far-field radio-frequency RF energy. The NeuralWISP is compatible with commercial RF identification readers and operates at a range up to 1 m. It includes a custom low-noise, low-power amplifier integrated circuit for processing the neural signal and an analog spike detection circuit for reducing digital computational requirements and communications bandwidth. Our system monitors the neural signal and periodically transmits the spike density in a user-programmable time window. The entire system draws an average 20 μA from the harvested 1.8-V supply.**

***Index Terms*—Brain machine interface, neural data acquisition, neural telemetry, radio-frequency identification (RFID), single–unit recordings, wireless sensor.**

I. Introduction

NEURAL interfaces have made tremendous technology-driven advances in the recent past. Cochlear implants are an early example of clinically relevant implantable devices [1], modern electronics are enabling previously impossible brain-research experiments [2], and major progress has been made toward neurally controlled prosthetics [3]. Since transcutaneous wiring poses a significant infection risk, it is desirable that a neural interface communicate and receive power wirelessly. Previous systems [4], [5] have achieved wireless operation by using a near-field inductive link to transmit power and data. However, these systems require that the external coil be located within a few centimeters of the internal coil. A wireless neural interface with a range of 1 m or more will enable the removal of the interrogator from the head and would allow wireless interfaces to be placed on small animals incapable of carrying the interrogator hardware, such as mice.

We present a wireless neural interface which harvests power from the radio-frequency (RF) energy provided by a standard commercial ultra-high frequency (UHF) radio-frequency-identification (RFID) reader. The system operates at a distance of up to 1 m from the reader. It records the spike count in a programmable window (typically 1–10 s) and subsequently transmits the spike count to the reader as part of the tag identification number that the reader is designed to acquire. This allows the neuroscientist a wireless, battery-free method of recording spike density $(spikes/second)$ as various tasks are performed or stimuli are presented.

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II. System Design

The NeuralWISP builds upon our prior work on the wireless identification and sensing platform (WISP) [6], [7]. The WISP is a fully-passive UHF RFID tag that uses an ultra-low power, general-purpose microcontroller (μC) for sensing, computation, and RFID communication. The use of a programmable μC allows WISP to be easily configured for different applications, including measurement of temperature, light level, strain, and acceleration [6]. These environmental sensor signals change slowly and, thus, permit periodic, low-frequency (1 to 50 Hz) measurement. However, a much faster sampling rate (at least 8 kHz) is necessary to detect neural spikes due to spectral content between 500 Hz and 2 kHz.

Achieving an 8-kHz sampling rate under the constraints of the limited power budget of an RFID tag is not possible with general-purpose microcontrollers available today. Instead, a continuous-time analog spike detector was designed to wake the system when spikes occur via a μC interrupt pin. This helps minimize average power consumption because the μC can remain in a low-power sleep mode during periods of inactivity and wake only to process spikes or communicate with the RFID reader. The μC counts spikes during a programmable window and is reset after the spike count is transmitted to the reader.

The architecture of the NeuralWISP is shown in Fig. 1. Like a typical RFID tag, power is received at the antenna, voltage-multiplied, rectified, and regulated to provide a stable system power supply. The neural input signal is amplified and applied to an analog spike detector in addition to an analog-to-digital converter (ADC) integrated in the μC. The μC performs the control and timing tasks, and implements the RFID communication protocol.

A. Power and Communication

NeuralWISP receives all of its power from the RFID reader. Commercial off-the-shelf (COTS) UHF RFID readers operating in the U.S. industrial-scientific-medical (ISM) band (902 MHz to 928 MHz) are limited in transmit power to the Federal Communications Commission (FCC) limit of 1 W (+30 dBm).

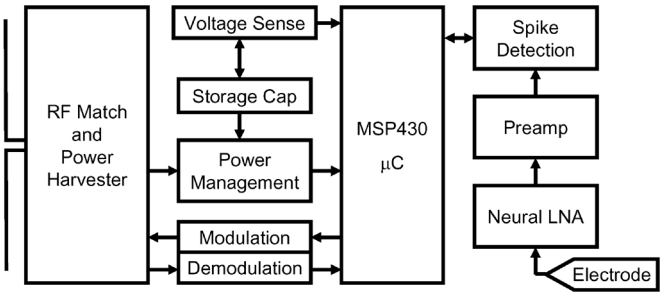

Fig. 1. Block diagram of NeuralWISP.

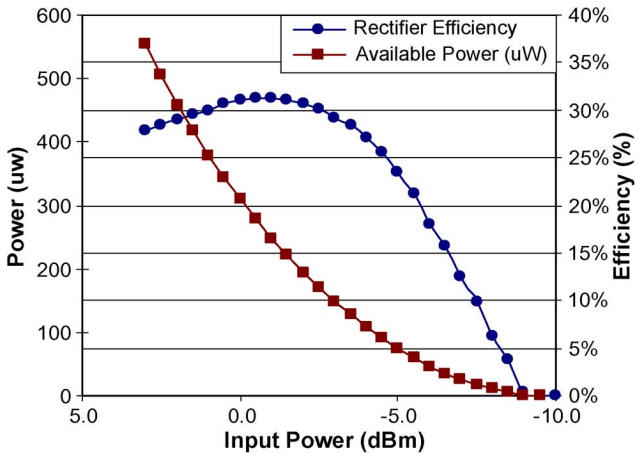

Fig. 2. Measured rectifier output power and efficiency versus input power. Estimating received power using Friis' Transmission Equation, an input power of +2.3 dBm corresponds to 1-m range for a typical UHF RFID system.

Readers often use an 8-dBi circularly polarized patch antenna, which has an approximate 60° beam width. Tags typically employ a 2-dBi dipole antenna. However, a number of factors decrease the power available to the tag. The most significant effect is path loss. Friis' Transmission Equation predicts that the amount of power received decreases with the square of wireless range. The circularly polarized reader antenna in conjunction with a (linearly polarized) dipole tag antenna also incurs 3-dB polarization loss. In addition, amplitude modulation (AM) in the downlink (reader-to-tag) and backscatter modulation in the uplink (tag-to-reader) communication causes up to 3-dB loss. Finally, tag rectifier efficiency, shown in Fig. 2, of about 25% causes 6-dB loss. All included, 427 μW (-3.7 dBm) is available after the rectifier at 1 m. Implantation causes additional losses due to dielectric constant mismatch at the air-tissue interface; however, experiments have demonstrated the feasibility of radiative power transfer in this regime [8].

The power and communication circuitry, shown in Fig. 3, are similar to that of conventional RFID tags, and [7] presents the design in detail. A five-stage voltage-multiplying rectifier converts the received RF signal from the reader into an unregulated voltage source for the tag, which is stored on C_{storage}. An L-match network transforms the tag impedance to match that of the antenna. The harvested voltage is converted to 1.8 V by a low-drop-out linear regulator with 1-μA quiescent current, which provides a stable supply voltage for the system. The

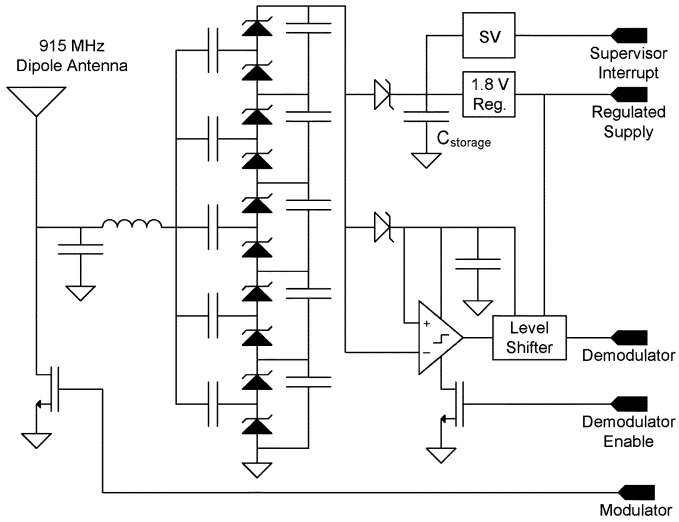

Fig. 3. Schematic of the RF front end including voltage-multiplying rectifier, modulator, demodulator with level shifter (LS), and voltage supervisor (SV). RF (low capacitance) Schottky diodes are filled black, and dc (low leakage) Schottky diodes are filled white. Also shown is the 1.8-V regulator, providing a stable supply for the rest of the system.

voltage supervisor provides a digital interrupt to wake the microcontroller while waiting for sufficient energy to operate.

NeuralWISP communicates by using the EPC Class 1 Generation 2 RFID protocol [9], allowing compatibility with industry-standard COTS readers. Downlink (reader-to-tag) communication is accomplished through reader AM. The demodulator employs a comparator to threshold the instantaneous received voltage against the average (minus a diode drop). A footer transistor disables the comparator to save 10 μA of quiescent current while communication is not needed. Uplink (tag-to-reader) communication is accomplished by modulation of the tag reflection coefficient. The modulator uses an RF transistor to short the antenna terminals together, thereby producing a strong reflected signal. In the worst case, approximately half of the nominal power is available to the tag due to reader AM and tag reflection modulation. Note that tag ID and memory communication errors are minimized through use of a 16-b CRC. Further details on the protocol can be found in [9].

B. Analog Signal Path

The extremely low signal levels recorded from neural probes place severe constraints on the analog front end. Input-referred noise levels must be $< 10\ \mu\text{V}_{\text{RMS}}$ while providing good linearity and high gain. These requirements frequently result in the low-noise neural amplifier consuming a majority of the system power. In the NeuralWISP, the power dissipation limits the wireless range, so power must be minimized. We designed a custom low-noise amplifier (LNA) in a 0.5-μm SOI BiCMOS process to meet these requirements. The amplifier is designed to provide 40-dB gain. A schematic is shown in Fig. 4.

The amplifier is built by using a two-stage op-amp with capacitive feedback, shown in Fig. 4(b). The midband gain is set to 100 by the ratio of the C_1 and C_2, which are 20 pF and 200 fF, respectively. Sizing the input capacitor C_1 presents a tradeoff between noise performance and chip area. Since large input transistors are used to minimize $1/f$ noise, the op-amp input ca-

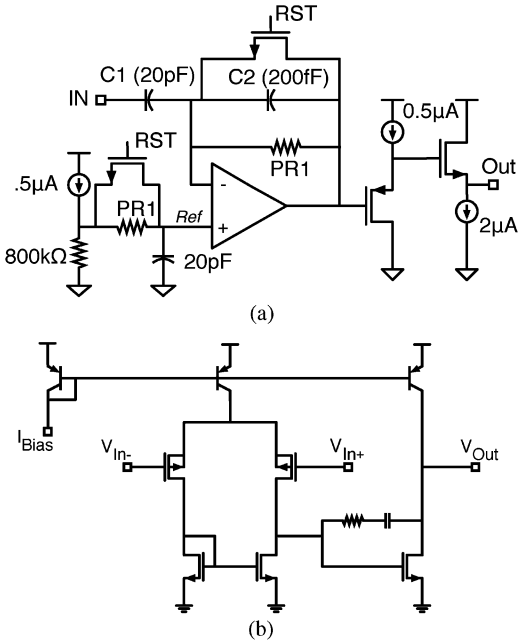

Fig. 4. (a) Schematic of custom 8-μA low noise neural amplifier fabricated in a 0.5-μm SOI CMOS process. (b) Schematic of the op-amp used in the low-noise amplifier.

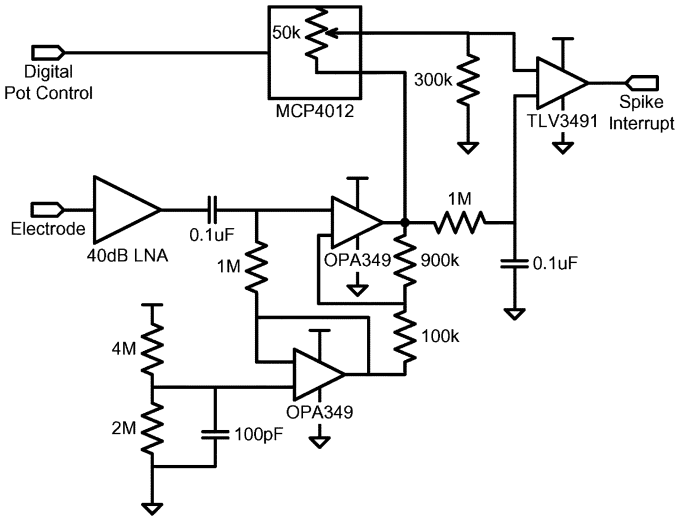

Fig. 5. Analog front-end circuitry, including custom 40-dB LNA, 20-dB postamp, and spike detector with programmable threshold. The 600-mV reference is generated by a voltage divider from the regulated 1.8-V supply and an opamp buffer. A noninverting opamp configuration provides the additional 20-dB gain. The spike detector compares the average (low-pass) signal to a programmable fraction of the instantaneous signal.

pacitance C_{opamp} is on the order of 1 pF. The input signal is attenuated by the capacitive divider formed by the C_1 and the op-amp. Since any attenuation before the op-amp will directly increase the input-referred noise, C_1 should be much larger than $C_{\rm opamp}$ to minimize attenuation. However, overly large values for C_1 would lead to an unnecessarily large chip area.

A closed-loop configuration was chosen for this system because open-loop amplifiers, while demonstrating superior noise efficiency factors (NEF), typically suffer from inferior power-supply rejection [10]. The LNA is ac coupled to reject dc offsets resulting from tissue-electrode interactions [11].

MOS-bipolar pseudoresistors [11] (PR) were used to set the dc bias point. The high-pass pole frequency is set by C_2 and the resistance of the PR. For small signals, the PRs have an incremental resistance of about 10^{12} Ω, resulting in a low-frequency pole below 1 Hz. The high-pass corner frequency set by the PRs is much lower than is necessary for the extra-cellular recording task being demonstrated here. However, all other options have significant drawbacks. A poly-silicon resistor would be prohibitively large, while transconductor implementations of high-valued resistors consume additional power and contribute noise. Previous amplifiers have used a subthrehold MOS transistor as a resistive element, but typically require a variable gate voltage to tune the resistance [12], [13]. Since the amplifier described here was designed to operate without any programming or configuration and was suitable for a variety of neural recording tasks targeting action potentials and field potentials, the PR was deemed to be a simple, flexible, and reliable method for setting the amplifier's dc bias point.

To avoid long settling times on power up due to the PRs, a power-on-reset circuit is included. When the reset signal is asserted, MOS switches temporarily short the PRs, allowing the amplifier to reach its equilibrium bias point quickly.

A source-follower output stage was chosen for its flexibility with respect to load conditions. A resistive load to ground will increase the current in the NMOS source follower transistor, allowing the amplifier to automatically adapt to resistive loads without consuming extra static bias current under lightly loaded conditions or using a complicated class AB output stage. A PMOS source follower is used to shift the output level up into the input range of the NMOS source follower, which drives the off-chip load. The LNA chip is completely self-contained, and includes a supply-independent bias current generator allowing consistent operation over a range of 1–5 V.

An additional gain of 20 dB is provided by a second amplifier built from two OPA349 opamps, shown in Fig. 5. The first opamp is used to establish a 0.6-V reference for ac coupling the amplifier stages. While the reference is derived from the supply, local regulation (see Fig. 3) ensures low-frequency stability and the 100-pF capacitor shunts high-frequency noise to ground. The second opamp is used in a noninverting gain configuration. The gain of the first stage allows relatively noisy micropower opamps to be used for the second gain stage. Consequently, the second stage consumes only 1.9 μA from a 1.8-V supply, including the reference.

The amplified signal is applied to an analog spike detector. Numerous algorithms for spike detection have been developed, ranging from simple thresholding detectors to sophisticated supervised learning classifiers, such as support vector machines (SVMs) [14]. Even with many other options available, the simple thresholding detector remains popular [4], [5]. An analysis of spike detection methods in the context of power constraints found thresholding on the absolute value to provide the best tradeoff between accuracy and computational requirements [15]. For this paper, a single-ended thresholding detector was found to have the appropriate combination of simplicity and efficacy.

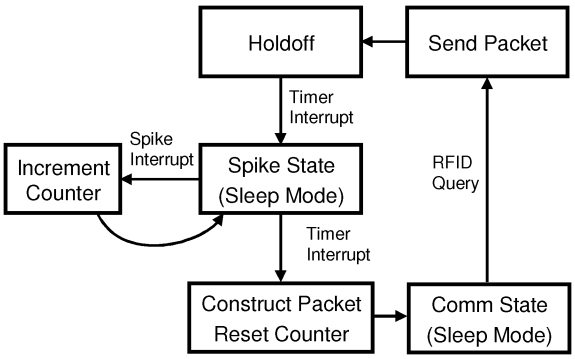

Fig. 6. Software state diagram. The μC is in the low-power Spike State for the majority of the time, awakening only to increment the spike counter after a detection or to communicate with the reader.

The signal is low-pass filtered with a time constant of 0.1 s to generate the detection threshold. Deriving the threshold from the amplified signal prevents any offsets in the opamps from corrupting the detection results. The signal is also shifted toward 0 V and attenuated by up to 15% via a variable-ratio resistive divider. A digitally controlled resistor, variable from $0\,\Omega - 50$ kΩ, determines the attenuation of the divider and thus the sensitivity of the spike detector. The shifted signal is compared to the low-pass-filtered signal to generate the detection signal, which triggers an interrupt in the μC. The spike detector's programmable threshold is set by the μC to a level stored in flash memory. The threshold level can be chosen by the user prior to deployment. Firmware control of the threshold also allows for future implementation of real-time adjustments to the threshold. These adjustments could be made based on the observed input or by including adjustment commands in the data sent from the reader to the NeuralWISP.

The output of the second amplifier is also connected to the ADC input of the MSP430 microcontroller to allow for direct digitization of the neural signal. The ADC has 10-b resolution and uses the supply as the reference. This provides a 1.76-mV LSB, or 1.76 μV input-referred.

C. Digital Control

An MSP430F2274 microcontroller (μC) is used to implement control, timing, and communication tasks. Fig. 6 shows the software architecture. On bootup, the μC configures the adjustable resistor in the spike detector. During the primary mode of operation, the μC will count spikes during a user-specified time interval (typically 1–10 s) and transmit the number of spikes detected at the end of the interval. During the counting interval, the μC is in a low-power sleep state for the majority of the time. The spike detector triggers an interrupt, which causes the μC to wake up, increment the spike count, and return to sleep. A timer drives another interrupt, which signals the end of the counting interval, causing the μC to exit the spike-counting mode and await a communication session with the reader. After communicating with the reader, the μC pauses for 3 s to allow the analog circuits to recover from RF interference that occurred during the read, then returns to the spike counting phase and repeats the cycle.

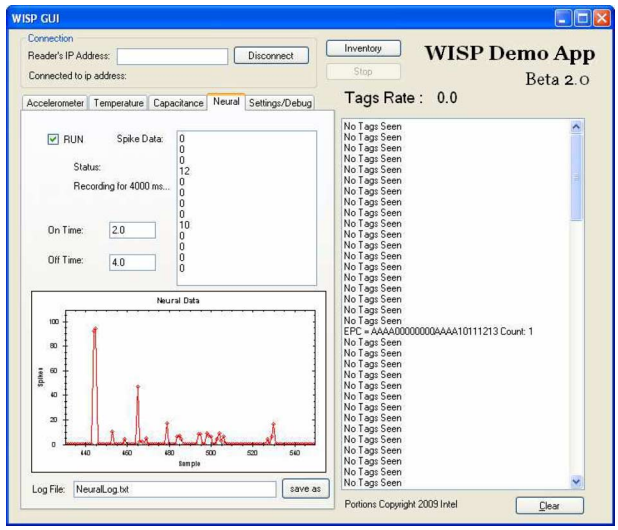

Fig. 7. Graphical user interface processes data from an Impinj Speedway RFID reader, displaying a graph of spike detections versus time.

D. Application Layer

A graphical user interface was developed to read, graph, and log spike density measurements reported by the NeuralWISP to the RFID reader. The application communicates via Ethernet using a low-level reader protocol (LLRP) [16]. A screen capture of the application in action is shown in Fig. 7.

The state cycle for the application begins by polling the reader until the NeuralWISP powers up and reports a spike count. Then, the application turns off the reader for a predetermined spike sampling period, which is set in the code of the NeuralWISP and in the application. During this time, the NeuralWISP counts spikes. After the sampling period has ended, the application again polls the reader. The NeuralWISP recharges and reports its spike count. The cycle then repeats. Note that the application stays synchronized with the NeuralWISP's charge-record-upload state cycle by waiting for the WISP to respond in the upload state. This ensures that timing errors do not accumulate over several iterations of the state cycle.

III. Test Results

The fabricated board is shown in Fig. 8. The populated board alone weighs 1.0 g, and a 900-MHz wire dipole antenna (not shown) weighs approximately 0.6 g. During spike counting, the system draws an average of about 20 μA of current from its unregulated supply, of which 8 μA is consumed by the neural LNA. A commercial RFID reader with +30-dBm transmitted power was used to wirelessly supply power and communicate with the NeuralWISP.

A. Analog Front End

The amplifier's noise was measured by using an HP 35670A dynamic signal analyzer with the input grounded. Fig. 10 shows the input-referred noise spectra at the output of the LNA and the post-amp, which was integrated from 0.5 Hz to 25 kHz and divided by the measured gain to find the input-referred rms noise voltage, which is 4.4 μV_{RMS} for the LNA. Even with the use of

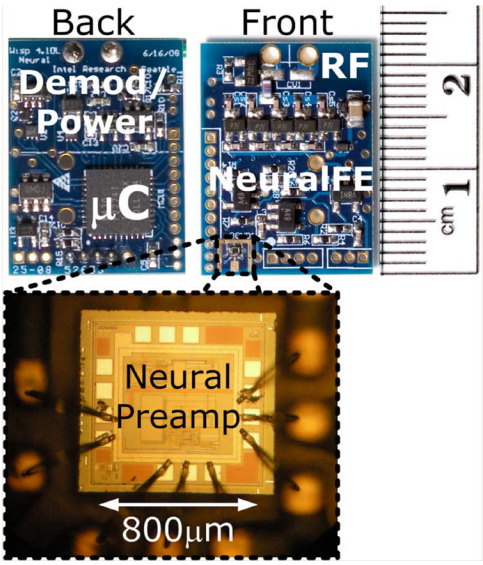

Fig. 8. System photograph. Inset shows chip-on-board mounting of the custom low-noise amplifier IC.

the micropower commercial opamps, it can be seen that the gain of the LNA suppresses the noise contribution of the postamp. In addition, very low-frequency noise is filtered by the ac coupling between the LNA and postamp.

The LNA can operate from a supply between 1 V and 5 V, and provides a measured gain of 39 dB with a bandwidth spanning from 0.5 Hz to 5.9 kHz. Operating from the NeuralWISP's regulated 1.8-V supply, the amplifier consumes 8 μA, including the bias generator and output buffer. Fig. 9 shows the measured frequency response of the first stage and the combined response of both gain stages. The LNA combined with the second amplifier provides a midband gain of 56 dB with a bandwidth from 2 Hz to 4.9 kHz. Table I shows a comparison of the LNA used here to other published neural amplifiers. The core amplifier has a current consumption of 3.3 μA, corresponding to an NEF of 4.0, which is comparable to other published amplifiers. Including buffering and bias generation, the total current is 8 μA, leading to an NEF of 6.2. It should also be noted that some of the amplifiers in the table [19], [20] are designed with much lower bandwidth for monitoring EEG signals or field potentials and, as a result, have lower current consumption. The NEF accounts for different bandwidths and noise levels, allowing comparison between amplifiers designed to different specifications.

B. Spike Detector

To characterize the spike detector, we applied a synthesized neural recording [14] to the NeuralWISP input. This technique allowed us to vary the signal-to-noise ratio (SNR) and spike rate in the recording and provide a reference to compare against our measured spike detection results in order to characterize the detector accuracy. Fig. 11 shows the operation of the detector on a single spike, with an 85 μV_{P-P} input signal. Software debouncing in the interrupt handler prevents any glitches in the spike detection signal from causing errors in the spike count.

Fig. 12 shows the spike detector accuracy. Spikes were detected by using the hardware analog spike detector (circle tick)

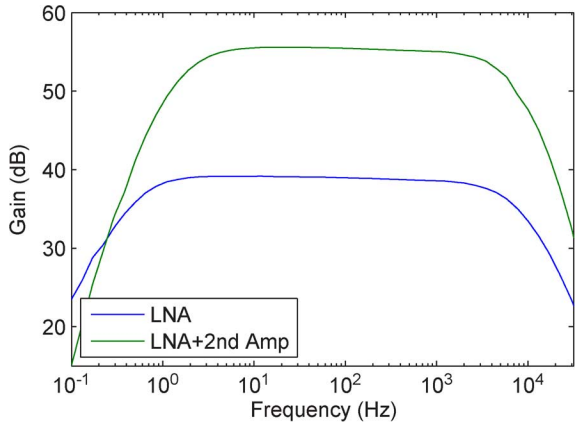

Fig. 9. Measured gain versus frequency for the low-noise amplifier (LNA, bottom), and the combined gain of the LNA and second amplifier.

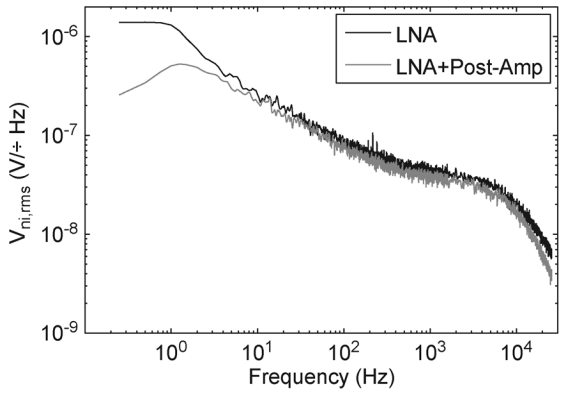

Fig. 10. Measured noise spectra at the output of the LNA and the postamp.

and by using a PC-based threshold-crossing detector (square tick) for comparison. Both detectors were run on synthetic recordings with an amplitude of approximately 400 μV_{P-P} and an SNR of 10 dB (left) and 6 dB (right). The results were compared with the known spike times provided by the signal synthesis software. The analog detector demonstrates comparable discriminative abilities to the software detector, indicating that noise contributions from the analog front end do not limit spike detection performance.

C. System Operation

Fig. 13 demonstrates the operation of the NeuralWISP. The middle trace is the unregulated voltage stored on a 100-μF capacitor C_{storage}, which begins at 0 V, since the WISP starts out without stored energy. Initially, the reader is configured to transmit power in continuous-wave (CW) mode, which charges the storage capacitor to 5.5 V where it is clamped by a Zener diode. As the stored voltage rises, the μC boots up (A). At point (B), continuous-wave transmission stops and the RFID reader reads data from the WISP. The first read following bootup will contain empty data. Following the read, the μC enters a 3-s waiting state (C) in order to allow the analog circuits to recover from RF interference which occurred during the read. After 3 s, the WISP begins counting spikes (D) for 5 s. After the spike-counting phase, the reader again transmits CW power (E) to recharge the storage capacitor, followed by another read,

TABLE I
COMPARISON OF NEURAL AMPLIFIERS

	Gain	I_{Amp}	NEF	$v_{ni,\,RMS}$	THD (@ Input)	PSRR	Bandwidth	Tech.
This Work[1]	39dB	3.3μA	4.0	4.4μV	0.2% @ 5mVpp	45dB	.5Hz-5.9kHz	.5μm
This Work[2]	39dB	8μA	6.2	4.4μV	0.2% @ 5mVpp	45dB	.5Hz-5.9kHz	.5μm
Holleman [17]	36.1dB	805nA	1.8	3.6μV	7.1% @ 1mVpp	5.5dB	.3Hz-4.7kHz	.5μm
Rai [18]	38.3	12.5μA	2.5	1.95μV	1% @ 1mVpp	63dB	.023Hz-11.5kHz	.13μm
Harrison [11]	39.5dB	16μA	4.0	2.2μV	1% @ 16.7mVpp	≥ 85dB	.025Hz-7.2kHz	1.5μm
Denison [19]	45.5dB	1.2μA	4.9	.93μV	—	—	.5Hz-250Hz	0.8μm
Wu [20]	40.2dB	330nA	3.8	.94μV	.053% @ 5mVpp	62dB	3mHz-245Hz	.35μm
Wattanapanitch [21]	40.9dB	2.7μA	2.7	3.1μV	1% @ 7.3mVpp	75dB	45Hz-5.3kHz	.5μm

[1]Core amplifier only
[2]Complete amplifier chip, including buffers reference and bias generation

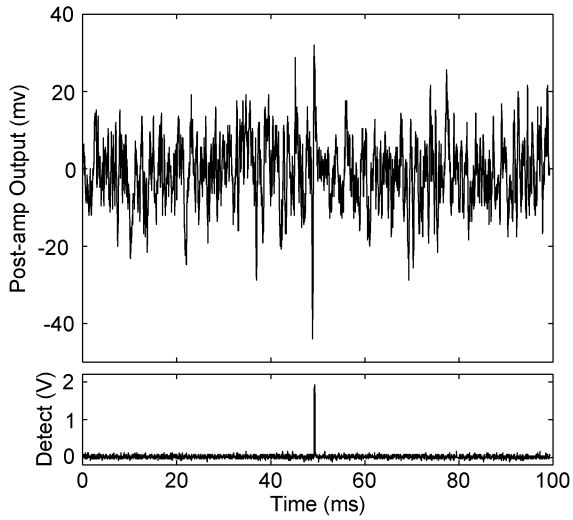

Fig. 11. Operation of the spike detector. The output of the postamp is shown at the top with an input signal containing a single spike with an SNR of approximately 10 dB. The amplitude at the input to the NeuralWISP is approximately 85 μV_{pp}.

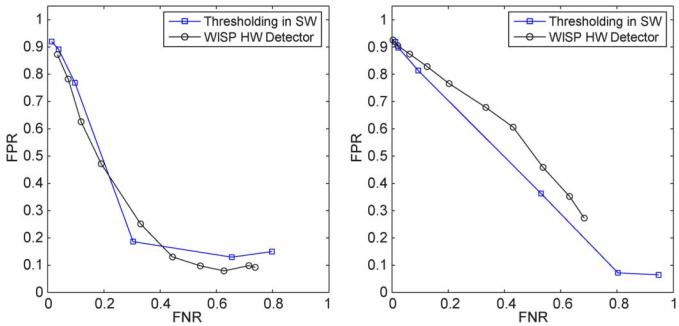

Fig. 12. Accuracy of the spike detector compared to a software spike detector for SNR = 10 dB (left) and SNR = 6 dB (right). The x axis is the false negative rate (FNR = number of missed spikes/number of total true spikes). The y axis is the false positive rate (FPR = number of false detections/number of total detections).

which retrieves data from the previous spike-counting phase (D). This cycle is repeated indefinitely.

The NeuralWISP's flexible hardware platform allows for many potential extensions to the present functionality. For example, it could be configured to sample spike waveforms after a spike is detected, and transmit the digitized data. An appropriate duty cycle would need to be chosen in order to meet the constraints imposed by the data rate allowed by

Fig. 13. Two read cycles of wireless operation, showing the spike detector output (top), the unregulated stored voltage (middle), and a microcontroller output (bottom) pulsed to show operation. The data were taken at a distance of approximately 1 m from the reader.

the tag/reader interface. Fig. 14 shows a spike captured and digitized by the NeuralWISP, where the digitization was begun in response to a detected spike. The digitized spike waveform is superimposed on the original waveform. This experiment was performed with wireless power, but the data were retrieved through a wired interface. It demonstrates that accurate reconstruction of a spike can be accomplished by waking the μC and ADC from low-power sleep after spike detection, dramatically reducing average system power. The digitization of detected events could also be used to implement a secondary screening of spikes in software, improving effective detection accuracy.

D. In-Vivo Results

To validate the NeuralWISP's ability to detect spikes *in vivo*, measurements of wing muscle activity from a Manduca Sexta moth were taken. Note that while the prototype NeuralWISP is too heavy to be carried by a moth, the integration of NeuralWISP onto an IC could allow in-flight measurements to be performed. Since the recording device is wirelessly powered, no batteries or wires are required. Since the battery consumes a large fraction of the weight budget of flying-insect-mounted electronics [22], a wirelessly powered interface would permit significant weight reduction compared to traditional sensing schemes. The setup is shown in Fig. 15, and a wirelessly powered recording captured by an oscilloscope is shown in Fig. 16.

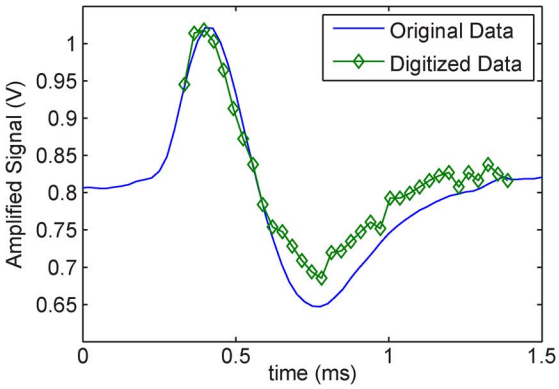

Fig. 14. Single spike digitized by the onboard ADC. The μC began sampling and converting in response to an interrupt from the spike detector.

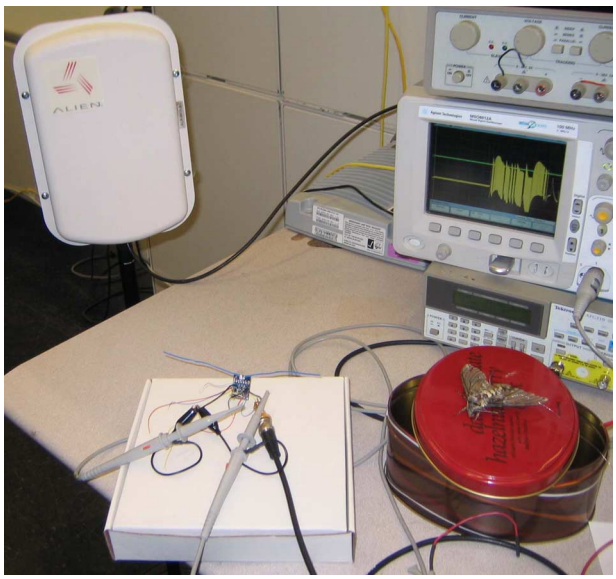

Fig. 15. *In-vivo* experiment setup showing a Manduca Sexta moth with tungsten wire electrodes in wing muscle tissue. The electrodes are connected to the NeuralWISP via a resistive attenuator. Spike density measurements are wirelessly recorded and communicated to the RFID reader.

NeuralWISP relies on extremely low-power custom analog front-end circuitry to allow operation from a wireless power source. In order to test the compatibility of the analog front end with an extra-cellular neural recording, we performed *in vivo* measurements on a macaque monkey (Macaca nemestrina). Fig. 17(a) shows spikes recorded with the NeuralWISP LNA and postamplifier, digitized with a standard rack-mounted acquisition system, and high-pass-filtered offline. The clean grouping of the spikes demonstrates that the NeuralWISP's analog front end has compatible input impedance and sufficient linearity to allow accurate recording of small neural signals in the presence of 60-Hz interference and local field potentials.

Fig. 17(b) shows the same spikes without the high-pass filtering. A combination of 60-Hz interference and low-frequency field potentials causes the spikes to be superimposed on a varying baseline level, complicating detection. For use in situations with significant low-frequency interference similar to that shown here, future systems should incorporate additional high-pass filtering. Fortunately, this filtering (and additional gain, if desired) can be easily implemented at a negligible cost in power using micropower opamps such as the one used for the postamp described before.

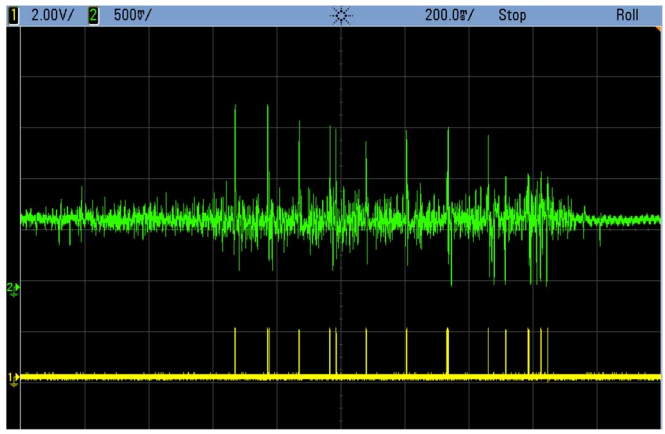

Fig. 16. Wirelessly powered data from wing muscle tissue captured over a 2-s timespan by an oscilloscope. The top trace shows the postamplifier output, which corresponds to approximately 2.4 mVpp at the input. The bottom trace shows the NeuralWISP spike detector output.

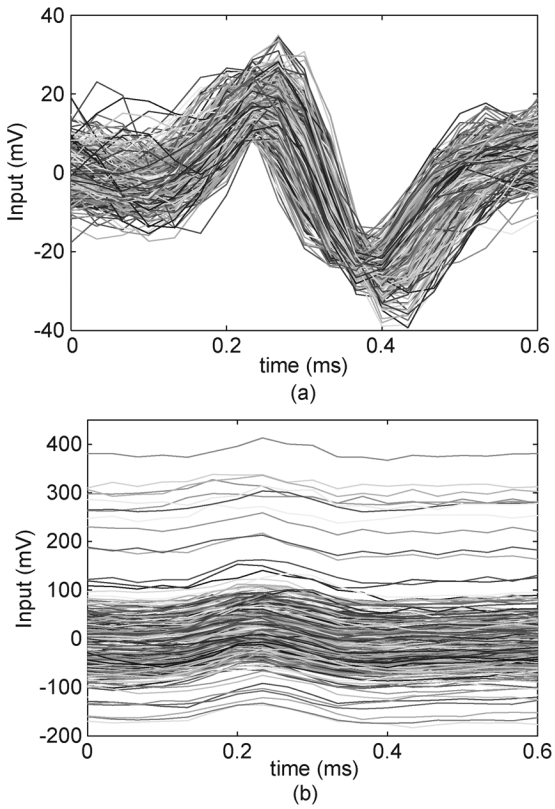

Fig. 17. Spikes recorded through the NeuralWISP's amplifiers and digitized with standard rack-mounted recording equipment. (a) High-pass-filtered spikes line up well. (b) Unfiltered data indicate a significant variation in the baseline.

IV. Discussion

There are a number of tradeoffs in the design of wirelessly powered neural recording systems. Some involve the use of the RFID protocol. RFID is a relatively mature technology, which provides a robust communication layer and low-cost (approximately U.S.$1000) interrogators. This enables wide-scale

deployment as well as collaboration with other researchers. Conversely, RFID technology was designed for reading many nodes once. In sensing applications, the goal is often to read one node repeatedly. This repurposing of the protocol constrains data throughput due to increased overhead. For example, the Gen2 protocol limits the query rate for 96-b tag IDs to about 1 kHz, which results in a maximum theoretical throughput of ∼100 kb/s. Reading tag memory increases throughput but decreases the tag-access rate to about 360 Hz for multibyte memory access. These estimates are based on 160-kb/s downlink and 640-kb/s uplink with preamble overheads, even bit distributions, and a single tag present (no singulation) [9]. However, NeuralWISP in its current implementation does not approach theoretical limits due to duty cycling of the reader. Specifically, 96 b are sent at an interval of 8-s plus tag charging time, which depends on the distance to the reader. At 1-m range, the charging time is approximately 3 s and, thus, the total period is 12 s. This low data rate necessitates a much distilled report of the recorded neural data, and at present, a spike count is reported.

Radiative energy transfer also has a number of tradeoffs. Advantages include the ability to power many nodes with one reader and transfer power over many wavelengths of distance (wavelength $\lambda = (c/f) = 0.33$ m for UHF RFID). Limitations on the number of nodes include shadowing (where one node blocks the reader signal from reaching a second node) and detuning (nodes in close proximity may detune the frequency band they are sensitive to). However, compared to other approaches, such as inductive coupling, radiative energy transfer enables operation at a much greater range. Disadvantages include low-power transfer efficiency and the necessity of an antenna on the scale of the RF wavelength. Low-power transfer efficiency, in turn, limits the features of the nodes due to power constraints. However, reductions in power consumption due to technology scaling are enabling increased functionality for the same power budget.

Finally, while one reader may power many tags, multiple readers in close proximity must time-multiplex. This is due to the tag demodulator design: simple peak detection lacks the ability to perform channel selection. Therefore, tags cannot selectively listen to one reader while other readers are transmitting simultaneously. This effectively means that tags in close proximity must share the communication bandwidth of one reader. Spike sorting, binning, and other forms of signal processing will allow maximum information to be gathered from a collection of nodes under the limited bandwidth constrains of one reader.

Wireless neural sensing inherently places an RF transmitter in close proximity to the signal to be detected. While pickup of 60-Hz noise can be greatly reduced due to the sensor being wirelessly interrogated, the radio can introduce interference in the measurement. In this paper, we separated the sensing and communication temporally, which places time gaps in the recording. In order to sense and communicate simultaneously, several techniques may help eliminate RF interference. First, integration of the electrodes, amplifiers, and spike detection circuitry to a size well below the RF wavelength helps prevent the electrodes from acting as an antenna. Second, integration of RF ejection filters in the signal path helps eliminate noise picked up by the electrode. Finally, shielding of the LNA and filters helps reduce direct interference from the amplifier.

As the NeuralWISP is currently configured, it measures spike density in a time window of a few seconds. While this is not the typical protocol for neuroscience experiments, it provides an indication of the activity level of the neuron being observed. This can provide useful information about sleep-wake state [23]. Simple measures of neural activity levels can also be used to gauge recovery from brain insult, such as that due to cardiac arrest. In [24], EEG was used to measure activity, but spike density could serve as another indicator. With additions to the firmware, even the modest data rate supported by the RFID protocol would allow other information to be transmitted, such as histograms of interspike intervals or spike amplitudes.

NeuralWISP enables a variety of interesting applications including monitoring of small animals and insects in laboratory environments as well as implantable neural sensors provided the device size is reduced through application-specific integrated-circuit (ASIC) integration. Similar applications for monitoring heart rate, blood sugar, blood pressure, etc. could leverage this technology by applying it to other biomedical sensors.

V. Conclusion

We have demonstrated a wirelessly powered neural interface with a range of 1 m. Using harvested RF power, the NeuralWISP transmits spike counts to a commercial RFID reader at user-programmable intervals. In addition to testing with simulation data, *in-vivo* measurements with a Manduca Sexta moth and macaque monkey validated the feasibility of this system in real-world conditions.

By operating from a wireless power source, the NeuralWISP allows indefinite operation without the need to change batteries, a critical need for implanted neural interfaces. The platform is also flexible and can be programmed to operate in different modes, such as spike time-stamp recording, or continuous recording on a duty-cycled basis. Future work reducing the size and weight of NeuralWISP will help lead to the practical deployment of wireless, battery-free neural recording systems.

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References

[1] R. P. Michelson, M. M. Merzenich, C. R. Pettit, and R. A. Schindler, "A cochlear prosthesis: Further clinical observations; preliminary results of physiological studies," *Laryngoscope*, vol. 83, no. 7, pp. 1116–1122, 1973.

[2] A. Jackson, J. Mavoori, and E. E. Fetz, "Long-term motor cortex plasticity induced by an electronic neural implant," *Nature*, vol. 444, pp. 56–60, 2006.

[3] D. M. Taylor, S. I. H. Tillery, and A. B. Schwartz, "Direct cortical control of 3d neuroprosthetic devices," *Science*, vol. 296, pp. 1829–1832, 2002.

[4] R. R. Harrison, P. T. Watkins, R. J. Kier, R. O. Lovejoy, D. J. Black, B. Greger, and F. Solzbacher, "A low-power integrated circuit for a wireless 100-electrode neural recording system," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 123–133, Jan. 2007.

[5] R. H. Olsson and K. D. Wise, "A three-dimensional neural recording microsystem with implantable data compression circuitry," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2796–2804, Dec. 2005.
[6] D. J. Yeager, A. P. Sample, and J. R. Smith, "WISP: A passively powered UHF RFID tag with sensing and computation," in *WISP: A Passively Powered UHF RFID Tag with Sensing and Computation*. Boca Raton, FL: CRC, 2008.
[7] A. P. Sample, D. J. Yeager, P. S. Powledge, and J. R. Smith, "Design of an RFID-based battery-free programmable sensingplatform," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 11, pp. 2608–2615, Nov. 2008.
[8] D. Halperin, T. S. Heydt-Benjamin, B. Ransford, S. S. Clark, B. Defend, W. Morgan, K. Fu, T. Kohno, and W. H. Maisel, "Pacemakers and implantable cardiac defibrillators: Software radio attacks and zero-power defenses," in *Proc. 29th Annu. IEEE Symp. Security and Privacy*, May 2008. [Online]. Available: http://www.secure-medicine.org/icd-study/icd-study.pdf
[9] EPCglobal, *Class 1 Generation 2 UHF Air Interface Protocol Standard,* 2009.
[10] J. Holleman and B. Otis, "A sub-microwatt low-noise amplifier for neural recording," in *Proc. IEEE 29th Annu. Int. Conf. Eng. Med. Biol. Soc.*, 2007, pp. 3930–3933.
[11] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.
[12] T. Horiuchi, T. Swindell, D. Sander, and P. Abshire, "A low-power CMOS neural amplifier with amplitude measurements for spike sorting," in *Proc. Int. Symp. Circuits and Systems*, 2004, vol. 4, pp. 29–32.
[13] P. Mohseni and K. Najafi, "A fully integrated neural recording amplifier with DC input stabilization," *IEEE Trans. Biomed. Eng.*, vol. 51, no. 5, pp. 832–837, May 2004.
[14] R. J. Vogelstein *et al.*, "Spike sorting with support vector machines," in *Proc. IEEE 26th Annu. Int. Conf. Engineering in Medicine and Biology Soc.*, 2004, vol. 1, pp. 546–549.
[15] I. Obeid and P. D. Wolf, "Evaluation of spike-detection algorithms for a brain-machine interface application," *IEEE Trans. Biomed. Eng.*, vol. 51, no. 6, pp. 905–911, Jun. 2004.
[16] EPCglobal, Low level reader protocol (LLRP). 2007. [Online]. Available: http://www.epcglobalinc.org
[17] J. Holleman and B. Otis, "A sub-microwatt low-noise amplifier for neural recording," in *Proc. IEEE 29th Annu. Int. Conf. Engineering Medicine and Biology Soc.*, 2007, pp. 3930–3933.
[18] S. Rai, J. Holleman, J. N. Pandey, F. Zhang, and B. Otis, "A 500 μW neural tag with 2 μVRMS AFE and frequency multiplying MICS/ISM FSK transmitter," in *Proc. IEEE Solid-State Circuits Conf., Digest Tech. Papers*, 2009, pp. 212–213.
[19] T. Denison, K. Consoer, A. Kelly, A. Hachenburg, and W. Santa, "A 2.2 μW 94 nV/$\sqrt{\text{Hz}}$ chopper-stabilized instrumentation amplifier for EEG detection in chronic implants," in *Proc. Int. Solid-State Circuits Conf. Digest of Tech. Papers*, 2007, pp. 162–594.
[20] H. Wu and Y. P. Xu, "A 1V 2.3 μW biomedical signal acquisition IC," in *Proc. IEEE Int. Conf. Digest Tech. Papers*, 2006, pp. 119–128.
[21] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 2, pp. 136–147, Jun. 2007.
[22] D. C. Daly, P. P. Mercier, M. Bhardwaj, A. L. Stone, J. Voldman, R. B. Levine, J. G. Hildebrand, and A. P. Chandrakasan, "A pulsed uwb receiver soc for insect motion control," in *Proc. IEEE Int. Solid-State Circuits Conf. Tech. Digest*, Feb. 2009, pp. 200–201.
[23] O. Y. Dergacheva, I. E. Khachikova, and A. A. Burikov, "Dynamics of neuron spike activity in the oral nucleus of the pons during the sleep-waking cycle in cats," *Neurosci. Behav. Physiol.*, vol. 34, no. 5, pp. 485–489, 2004.
[24] X. Jia, M. A. Koenig, R. Nickl, G. Zhen, N. V. Thakor, and R. G. Geocadin, "Early electrophysiologic markers predict functional outcome associated with temperature manipulation after cardiac arrest in rats," *Crit. Care Med.*, vol. 36, no. 6, p. 1909, 2008.

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