A Current-Reuse Complementary-Input Chopper-Stabilized Amplifier for Neural Recording

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***Abstract*—This paper presents a current-reuse complementary-input (CRCI) telescopic-cascode chopper stabilized amplifier with low-noise low-power operation. The current-reuse complementary-input strategy doubles the amplifier's effective transconductance by full current-reuse between complementary inputs, which significantly improves the noise-power efficiency. A pseudo-resistor based integrator is used in the DC servo loop to generate a high-pass cutoff below 1 Hz. The proposed amplifier features a mid-band gain of 39.25 dB, bandwidth from 0.12 Hz to 7.6 kHz, and draws 2.57 μA from a 1.2-V supply and exhibits an input-referred noise of 3.57 μV_{rms} integrated from 100 mHz to 100 kHz, corresponding to a noise efficiency factor (NEF) of 2.5. The amplifier is designed in 0.13 μm 8-metal CMOS process.**

I. INTRODUCTION

There is a rapid development of miniature implantable integrated neural recording systems, which allow neuroscientists and clinicians to treat neurological disorders, such as epilepsy, Parkinson's disease, and spinal cord injuries. Recording brain neural activity facilitates diagnosis. In order to simultaneously record and stimulate at multiple sites in the brain, multi-electrode recording systems are needed [1]. For such applications, a large number of neural amplifiers (one per active electrode), are incorporated in the recording systems. Thus, constraints of power and chip area are placed on the neural amplifiers. The low-power low-voltage operation is essential to avoid thermal damage to surrounding tissues, preserve long-battery life, and enable wirelessly-delivered or harvested energy supply. Besides, because the bioelectrical signals are so weak, the input-referred noise of the amplifier should be lower than the typical extracellular neural background noise of 5-10 μV_{rms} to get clean neural signal recordings. Moreover, large DC offset which can occur at the electrode-tissue interface due to the polarization of bio-potential gel-electrodes requires offset cancellation or AC-coupling. Lastly, sufficient common-mode and power-supply rejection is needed to reject the inevitable interference and supply noise.

Recently, pioneering low-power low-noise CMOS bio-potential amplifiers [2]-[9] have been reported. The strategy of sizing the input devices relatively large [2]-[5] was utilized to reduce *1/f* noise, which requires large on-chip dc-coupling capacitor (C_{in}). Chopper stabilization technique is efficient in suppressing *1/f* noise with minimal signal or noise aliasing, and has been widely used in bio-potential amplifier development [6]-[8]. The capacitively-coupled chopper topology with a DC servo-loop introduced in [6] can reject DC offset at the electrode-tissue interface. To realize chopper stabilization, two sets of CMOS switches were added to a folded-cascode amplifier [6]. However, compared with the telescopic-cascode amplifier, the folded-cascode amplifier has additional current branches, and is not power-efficient. Although telescopic-cascode amplifier has less common-mode input range and output swing, the small signal levels of neural signals relax those requirements. Furthermore, the standard SC integrator used in [6] requires a very large capacitor to obtain a high-pass cutoff below 1 Hz, which significantly increases the chip area.

In this paper, a current-reuse complementary-input (CRCI) telescopic-cascode chopper stabilized amplifier is proposed. The CRCI strategy fully reuses the current, which results in doubling the amplifier's effective transconductance at the same bias current. This strategy significantly improves the noise-power efficiency, and also doubles the amplifier's open-loop gain. In the DC servo loop, pseudo-resistors that exhibit large-valued resistance [2] and small area, are employed in the integrator, which significantly reduces capacitor size requirement to achieve a sub-Hz high-pass cutoff.

II. DESIGN OF CURRENT-REUSE COMPLEMENTARY-INPUT (CRCI) CHOPPER-STABILIZED AMPLIFIER

A. Amplifier Top-Level Design

Fig.1 shows the configuration of the proposed chopper-stabilized amplifier. This capacitively-coupled chopper stabilization topology with a DC servo loop is composed of a chopper stabilized amplifier (OTA G_m, *CH1*, and *CH2*), a DC feedback (*PR* and *CH3*) biasing the OTA input, a capacitive feedback network (C_{in}, C_{fb}, and *CH3*), and a DC servo loop (an integrator, PMOS-buffer, C_{hp}, and *CH4*). Fully differential architecture is employed to provide high common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR). The mid-band gain of the amplifier is set by on-chip capacitor ratio C_{in}/C_{fb}, which features excellent noise and linearity properties. With *CH1* employing complementary switches, a rail-to-rail input common mode range is achieved due to the input capacitor (C_{in}). The input impedance of the amplifier is $1/(2 \cdot f_{chop} \cdot C_{in})$, where f_{chop} is the chopping frequency.

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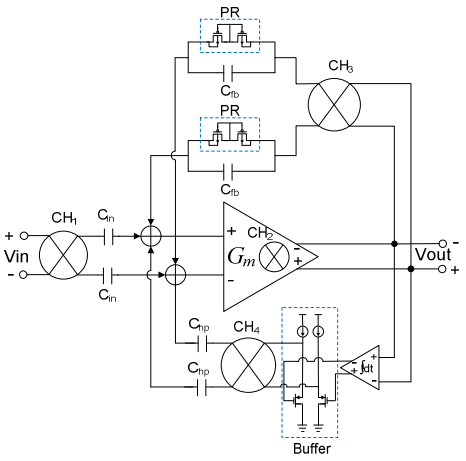

Fig. 1. Configuration of the proposed chopper-stabilized amplifier.

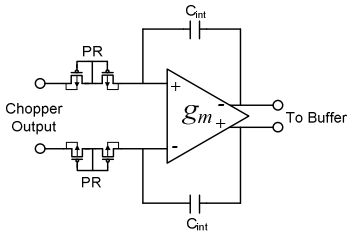

Fig. 2. Configuration of the pseudo-resistor based integrator.

The DC servo loop defines the high-pass cutoff characteristics of the amplifier to reject large DC electrode offset. The DC signal at the output of the chopper amplifier is amplified by the integrator, and up-modulated to chopping frequency by *CH4*. Then, this up-modulated signal is fed back to the input of the chopper amplifier through capacitor C_{hp} to cancel out the up-modulated DC electrode offset by negative feedback. The combination of *CH4* and C_{hp} can be seen as an equivalent impedance of $1/(2 \cdot f_{chop} \cdot C_{hp})$ that loads the integrator's output, which may lead to a large drop of the integrator's DC gain. Two PMOS source-follower buffers are employed to isolate the integrator's output and the switch capacitor load, instead of using a fully-differential opamp buffer. PMOS source-follower exhibits the properties of better noise performance, less power consumption, and smaller area. The more important reason is the source-follower introduces less parasitic poles, which would not degrade the loop stability. The chopped amplifier [6] employed a SC integrator which required a very large capacitor to obtain a high-pass cutoff below 1 Hz, which was not area-efficient. Pseudo-resistors feature extremely high incremental resistance (>10^{11} Ω) with small voltages (< 0.2 V) across them. Fig.2 shows the configuration of the pseudo-resistor based integrator. In our design, pseudo-resistors are used to generate a sub-Hz high-pass cutoff instead of the SC resistors, which significantly saves the chip area. The high-pass cutoff is given by [6]:

$$f_{hp} = \frac{C_{hp}}{C_{fb}} \cdot \frac{1}{2\pi R_{\text{int}} C_{\text{int}}} \quad (1)$$

where R_{int} is the equivalent resistance of the pseudo-resistors. Current-mirror OTA is used in the integrator to achieve wide output swing. The details are not critical to the operation of the design and will not be presented here.

The input-referred noise of the chopper stabilized amplifier can be expressed as [6]:

$$V_{ni,chop-amp} = \frac{C_{in}+C_{hp}+C_{fb}+C_{OTA}}{C_{in}} \cdot V_{ni,OTA} \quad (2)$$

where C_{OTA} and $V_{ni,OTA}$ represent the input capacitance and the input-referred noise of the OTA G_m, respectively.

B. CRCI Telescopic-Cascode OTA Design

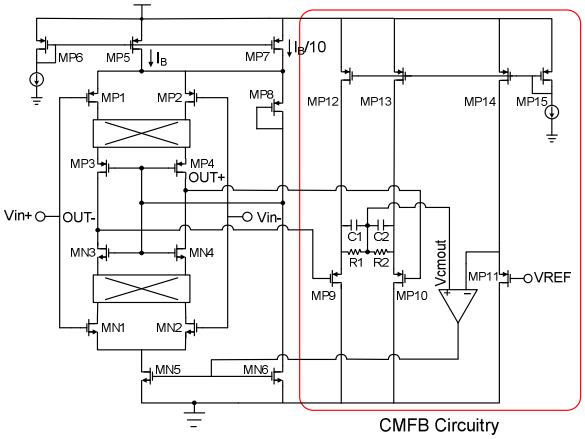

Fig. 3. Configuration of the complementary-input telescopic amplifier.

Fig.3 shows the schematic of the proposed current-reuse complementary-input (CRCI) telescopic-cascode OTA. Compared with the folded-cascode OTA used in [6]-[8], telescopic-cascode OTA is more noise-power efficient while keeping high open-loop gain feature, because it has fewer current branches. The telescopic-cascode topology has narrower output swing, but by properly choosing the closed-loop gain (around 40 dB) its output swing is sufficient for the neural amplifiers, due to the small signal levels of the neural signals. In our design, a CRCI telescopic-cascode OTA is employed. By driving the gates of both PMOS and NMOS input transistors, the CRCI [5] fully reuses the current and doubles the effective transconductance, which leads to a significant reduction in input-referred noise. Instead of providing separate bias for the gate of the complementary-input transistors [5], the gates of the complementary-input pairs are tied together (*MP1-MN1*, and *MP2-MN2*), respectively, which saves one bias reference and simplifies the design. In [5], a two-stage Miller-compensated structure was employed to achieve sufficient open-loop gain. The power consumption of the second stage can be minimized to achieve low power. However, the strategy needs large compensation capacitor to ensure stability, which leads to small bandwidth product. Thus, higher chopping frequencies are not allowed to

minimize the *1/f* noise. In our design, Cascode PMOS (*MP3* and *MP4*) and NMOS (*MN3* and *MN4*) pairs are utilized to increase the open-loop gain. A diode-connected transistor (*MP8*) and current source (*MP7*) are employed to bias the gates of the cascode transistors. Complementary switches are placed at the low impedance node in between the drains of input transistors and the sources of the cascode transistors, which allows chopping the amplifier at higher frequencies. Voltage-buffer CM-sense circuitry is used to avoid the loading effect from *R1* and *R2*. Capacitors *C1* and *C2* are added in parallel with each sense resistor to compensate the CMFB loop by introducing a left-half-zero.

TABLE I
TRANSISTOR PARAMETERS OF CURRENT-REUSE COMPLEMENTARY-INPUT TELESCOPIC-CASCODE OTA

Transistors	W/L (μm)	Id (μA)	g_m/I_d (V^{-1})
MP1,2	15.2/0.45	0.8	23
MN1,2	48/2	0.8	27
MP3,4	12/1	0.8	22.93
MN3,4	16/1	0.8	32
MP6,7	2.4/0.8	0.16	21
MP5	24/0.8	1.6	20.78
MN5	20/1	1.6	24.75
MN6	2/1	0.16	25.1
MP8	8/6	0.16	18.96
MP9,10,11	2.4/0.4	0.09	25.3
MP12,13,14	8/0.6	0.09	24.7
MP15	4/0.6	0.045	24.7

Thick-oxide MOS transistors are used at the complementary-input to reduce gate leakage currents that could result in significant DC-offsets, and to offer higher intrinsic gain. The complementary-input transistors are biased in sub-threshold region to improve the noise-power efficiency [2]. Other transistors are also carefully sized for reduced noise and proper bias, as shown in Table I.

For the CRCI telescopic-cascode OTA, the primary noise sources are the complementary-input pairs (*MP1,2* and *MN1,2*). It should be mentioned the *1/f* noise of the cascode transistors (*MP3,4* and *MN3,4*) is not up-modulated, since the switches are placed at the sources of cascode transistors (low impedance node) instead of the output node (high impedance node). Thus, although the noise contribution of cascode transistors is significantly attenuated, the relatively large gate area is required to minimize their *1/f* noise.

The input-referred thermal noise of the CRCI telescopic-cascode OTA can be approximated as:

$$V_{ni,OTA}^2 = [\frac{16kT}{3} \cdot \frac{1}{g_{mp1}+g_{mn1}}] \cdot \Delta f \qquad (3)$$

where g_{mp1} and g_{mn1} represent the transconductance of input PMOS (MP1,2) and NMOS (MN1,2), respectively.

If $g_{mp1} = g_{mn1} = g_m$, then the equation (3) is simplified as:

$$V_{ni,OTA}^2 = [\frac{16kT}{3} \cdot \frac{1}{2g_m}] \cdot \Delta f \qquad (4)$$

The input-referred thermal noise of a basic differential-pair operational amplifier can be expressed as:

$$V_{ni,th}^2 = [\frac{16kT}{3} \cdot \frac{1}{g_m}] \cdot \Delta f \qquad (5)$$

Comparing the equations (4) and (5), the amplifier transconductance is doubled by the CRCI strategy at the same bias current.

To compare the power-noise tradeoff among amplifiers, the noise efficiency factor (NEF) [2] is adopted:

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \qquad (6)$$

where k is boltzmann constant, U_T is the thermal voltage, $V_{ni,rms}$ is the total input-referred noise, I_{tot} is the total supply current, and BW is the -3 dB bandwidth of the amplifier.

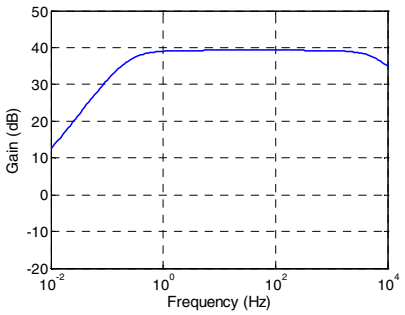

Fig. 4. The simulated transfer function of the chopper stabilized amplifier.

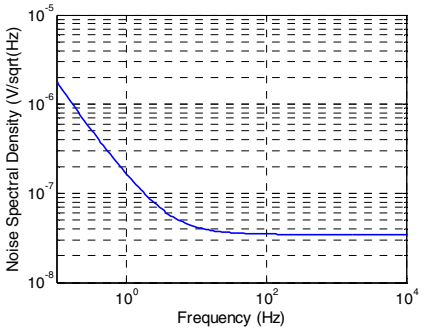

Fig. 5. The simulated input-referred noise spectrum of the chopper stabilized amplifier.

III. SIMULATION RESULTS

Our proposed amplifier is designed in 0.13 μm 8-metal CMOS process. The amplifier draws a total current of 2.57 μA (including the dynamic current from the chopper switches) from a power supply of 1.2 V. The chopping frequency is 75 kHz. C_{in} and C_{fb} are chosen to be 2 pF and 20 fF, respectively, which set an ideal closed-loop gain of 100 (40 dB). The calculated input impedance by $1/(2 \cdot f_{chop} \cdot C_{fb})$ is 3.3 *MΩ*.

The simulated transfer function of the amplifier is shown in Fig. 4. The mid-band gain of the chopper stabilized amplifier is 39.25 dB. The pass-band is from 0.12 Hz to 7.6 kHz. Due to the use of the pseudo-resistors, the capacitor (C_{int}) used in the integrator is 15 pF, which is much smaller than the

TABLE II
NEURAL RECORDING AMPLIFIERS PERFORMANCE COMPARISON

	[3] BioCAS '07	[5] BioCAS '12	[6] JSSC '07	[7] JSSC '11	[8] ISCAS '12	This work
Process (μm)	0.5	0.13	0.8	0.065	0.13	0.13
Current (μA)	2.7	12.1	1	2.1	0.9	2.57
Vdd (V)	2.8	1	1.8 to 3.3	1	1.2	1.2
Gain (dB)	40.85	40	41	40	40-83	39.25
BW (Hz)	45~5.32k	.05-10.5k	0.05-180	0.5-100	340-7.5k	0.12-7.6k
Input-referred thermal noise (nV/sqrt(Hz))	31	/	100	60	64.9	34.6
$V_{ni,rms}$ (μV)	3.06	2.2	0.98	6.7	2.06	3.57
NEF	2.67	2.9	4.6	3.55*	3.28	2.5
$NEF^2 \cdot Vdd$	20	8.4	38	12.6	12.9	7.5
CMRR (dB)	66	80	> 100	> 110	/	> 68
PSRR (dB)	75	≥ 80	/	120	/	> 65

*NEF is estimated as 3.55, since enabling DC servo loop to generate high-pass corner increases the current consumption from 1.8 μA to 2.1 μA, while assuming DC servo loop not contributing any noise.

capacitor in [6]. Fig. 5 shows the input-referred noise spectrum of the amplifier. The input-referred thermal noise density is about $34.6\,nV/\sqrt{Hz}$. The total input-referred noise integrated from 100 mHz to 100 kHz is 3.57 μV_{rms}. Our calculated NEF from [6] is 2.5. Fig. 6 and 7 show the Monte Carlo simulation of CMRR and PSRR, respectively. The worst-case CMRR and PSRR are better than 68 dB and 65 dB, respectively.

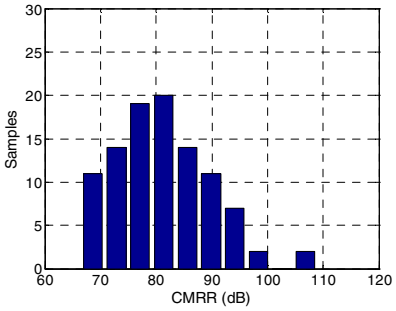

Fig. 6. Monte Carlo simulation of CMRR (100 runs).

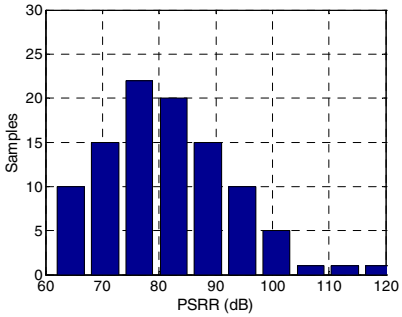

Fig. 7. Monte Carlo simulation of PSRR (100 runs).

Our proposed amplifier is compared with a few other state-of-the-art neural recording amplifiers in Table II. Our amplifier achieves the best NEF of 2.5. Because the conventional NEF does not consider the supply voltage, a modified metric $NEF^2 \cdot VDD$ reported in [9] is also calculated. The $NEF^2 \cdot VDD$ of our amplifier is 7.5.

CONCLUSION

A novel CRCI telescopic-cascode chopper stabilized amplifier for neural recording is presented. By utilizing the CRCI telescopic-cascode OTA, the noise-power efficiency is significantly increased. Pseudo-resistors are employed to implement the integrator in the DC servo loop to generate a sub-Hz high-pass cutoff, which significantly relaxes the capacitor size requirement and saves chip area in standard SC-integrator. Our amplifier achieves an input-referred noise of 3.57 μV_{rms} integrated from 100 mHz to 100 kHz, corresponding to a noise efficiency factor (NEF) of 2.5.

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