A High Input Impedance Low-Noise Instrumentaion Amplifier with JFET Input

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***Abstract*—This paper presents a high input impedance instrumentation amplifier with low-noise low-power operation. JFET input-pair is employed instead of CMOS to significantly reduce the flicker noise. This amplifier features high input impedance (15.3 GΩ||1.39 pF) by using current feedback technique and JFET input. This amplifier has a mid-band gain of 39.9 dB, and draws 3.65 µA from a 2.8-V supply and exhibits an input-referred noise of 3.81 μV_{rms} integrated from 10 mHz to 100 kHz, corresponding to a noise efficiency factor (NEF) of 3.23.**

I. INTRODUCTION

There is a great need of low-noise low-power bio-potential amplifiers, which is able to amplify signals ranging from mHz to kHz. The signals from human or animal subjects are coupled through an electrode interface, which can be modeled as a capacitor in series with a resistor [1] or a capacitor in parallel with a resistor [2]. The source impedance of the electrode interface may interact with the input impedance of the amplifier, resulting in voltage dividers or parasitic frequency corners, and attenuating the bio-signal to be measured. In order to avoid this attenuation, a bio-potential amplifier with high input impedance is desired.

Recently, pioneering low-power low-noise CMOS bio-potential amplifiers [3]-[5] have been reported. As illustrated in Fig.1, these amplifiers employed capacitive feedback technique around an operational transconductance amplifier (OTA) to determine the closed-loop gain, and used MOS-pseudoresistors (PRs) to create a low-frequency high-pass corner. To minimize flicker noise, PMOS transistors with large gate area had to be adopted as the input devices, leading to a large input capacitance of the OTA (C_{in}). However, since C_{in} contributed to the noise gain, the increase of C_{in} increases the overall input-referred noise [3]. In order to minimize the effect of C_{in} on noise performance, C_1 must be made much larger than C_{in}. And C_1 may be large enough that input signals are significantly attenuated by the capacitive divider formed by C_1 and the equivalent capacitance of the electrode interface. And a parasitic low-frequency low-pass pole may be generated by C_1 and the equivalent resistance of electrode interface, filtering out the signals of our interest. BJTs and JFETs transistors exhibit much lower flicker noise than MOS transistors [6], but they cannot be used as the input devices in the configuration shown in Fig.1. The base or gate current would have to flow through the PRs, this bias current raises the low-cutoff frequency by lowering the incremental resistance of the PRs, and causes a large voltage drop across it, disrupting the bias of the OTA.

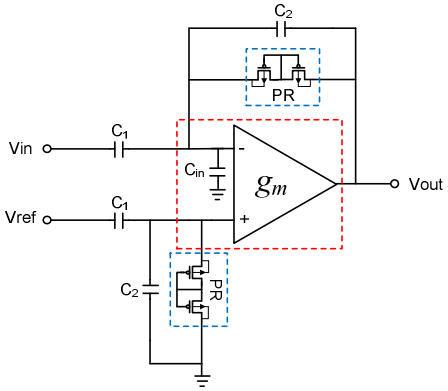

Fig. 1. Configuration of the capacitive-feedback bio-potential amplifier.

Chopper stabilization technique has been used to suppress flicker noise in instrumentation amplifiers [1], [7], [8]. In [1], by using ac modulation in the input and feedback paths, the gain of the amplifier was set by capacitive feedback with excellent noise and linearity performance. However, the chopping amplifier with capacitive feedback exhibits a reduced input resistance. This input resistance may be small enough to significantly attenuate the input signals when interfaced with a resistive electrode, or generate a parasitic high-pass corner with a capacitive electrode interface and filter out the signals of our interest. Besides, due to the up-modulated offset in chopper stabilization technique, additional techniques such as ripple reduction loop (RRL) [7] and auto correction feedback (ACFB) [8] are need to suppress the significant ripple at the amplifier output, which reduces the noise-power efficiency of the amplifier.

In this paper, a high input impedance instrumentation amplifier with low-noise low-power operation is proposed. It utilizes JFET as the input device to provide much higher input impedance than BJT and much lower noise than MOSFET. Besides, the closed-loop gain is set by current feedback technique [9] and an additional feedback path provided by sensing terminals, instead of capacitive feedback [3], for maintaining high input impedance. Several strategies, such as active cascode technique and emitter degeneration current source, are utilized to enhance the noise-power efficiency. In addition, noise is analyzed, and methods of noise optimization are given.

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II. DESIGN OF HIGH INPUT IMPEDANCE LOW-NOISE INSTRUMENTATION AMPLIFIER

A. Overall Design

Fig. 2(a) shows the configuration of the proposed instrumentation amplifier composed of feedback resistors and an operational amplifier (*OPA*) with sensing terminals (*Sense−,+*). The sensing terminals provide an additional signal path for feedback to achieve a high impedance for bio-potential inputs (*Vin−,+*). The schematic of the OPA is shown in Fig. 2(b). The *OPA* consists of two stages to provide sufficient open-loop gain. The first stage is a differential amplifier with four input terminals for bio-potential and feedback sensing. At the second-stage, we used two single-ended amplifiers instead of a differential structure. The advantage is that only one common-mode feedback circuitry (CMFB) is needed to set the bias of the outputs for both stages, while keeping our amplifier fully differential. This approach not only reduces the design complexity, but also saves power and chip area.

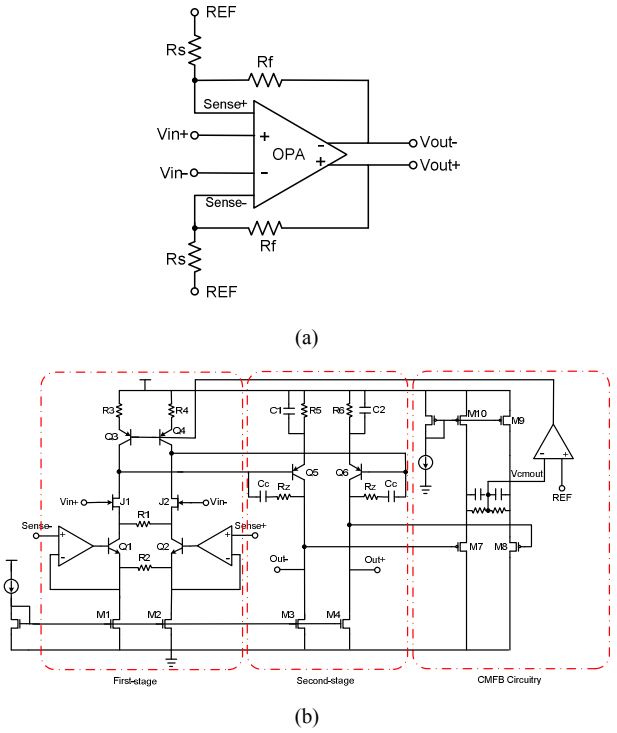

Fig. 2. (a) The configuration of the proposed instrumentation amplifier. (b) The schematic of the operation amplifier (OPA) with sensing terminals.

The instrumentation amplifier used the current feedback technique [9] and the resistive feedback through the sensing terminals to set the closed-loop gain. The current feedback loop is formed by R_1 and R_2. The differential voltage on sense terminals *Sense−,+* is applied across R_2 by the active cascode formed by $Q_{1,2}$ and the auxiliary amplifiers (*Aaux*). The current flowing through R_2 generates a voltage drop across R_1, which is summed to the input signals *Vin−,+* at the sources of the input pair. The feedback factor of this current feedback loop can be expressed as:

$$\beta_1 = \frac{R_1}{R_2\left(1+\frac{2}{g_{mQ1}\cdot A\cdot R_2}\right)} \tag{1}$$

where g_{mQ1} is the transconductances of the transistors Q_1 and Q_2, and A is the open-loop gain of the auxiliary amplifier. The auxiliary amplifier increases the effective transconductance by A and largely reduces the impedance seen at the emitters.

If the $g_{mQ1}A$ is large enough ($g_{mQ1}\cdot A \gg \frac{2}{R_2}$), the feedback factor can be simplified to:

$$\beta_1 = \frac{R_1}{R_2} \tag{2}$$

By using the active cascode technique, the values of R_1 and R_2 for accurately setting the feedback factor β_1 are significantly reduced at a given feedback factor in low-current operation. Thus, area and parasitic capacitances associated with R_1 and R_2 is reduced. Moreover, the noise performance is improved if the value of R_1 is reduced, because R_1 is at the source of the input JFET, any noise from R_1 would be directly referred to the input without any attenuation.

Emitter degeneration is employed to implement the current source loads to reduce its effective transconductance. By using this technique, the noise contribution from the current source loads can be significantly reduced. In addition, the first-stage open-loop gain would increase due to the increase of the output resistance of current source load, and the matching is also improved.

The feedback resistors R_f and Rs add extra attenuation of the output feedback to the *Sense* terminals. Since the open-loop voltage gain of the two stages combined is large enough, the closed-loop gain of the instrumentation amplifier can be expressed as:

$$A_{CL} = \frac{R_2}{R_1}\left(1+\frac{R_f}{R_s}\right) \tag{3}$$

B. Noise Analysis of the Instrumentation Amplifier

The overall input-referred noise of the instrumentation amplifier can be expressed as:

$$V_{ni}^2 = V_{ni,OPA}^2 + \frac{(4kTR_s\cdot\Delta f)\left(\frac{R_f}{R_s}\right)^2}{A_{CL}^2} + \frac{4kTR_f\cdot\Delta f}{A_{CL}^2} \tag{4}$$

where $V_{ni,OPA}$ is the input-referred noise of the OPA, and A_{CL} is the closed-loop gain of our instrumentation amplifier. In our design, the closed-loop gain A_{CL} is around 40 dB. By properly choosing the resistance of R_s and R_f, and the ratio of them, the noise contribution from these resistors is negligible compared to the input-referred noise of the OPA. The equation (4) could be simplified as:

$$V_{ni}^2 = V_{ni,OPA}^2 \quad (5)$$

The input-referred noise from the OPA can be calculated as:

$$V_{ni,OPA}^2 = V_{ni,first}^2 + \frac{V_{ni,sencond}^2}{A_{OL,first}^2} \quad (6)$$

where $V_{ni,first}$ and $V_{ni,\mathrm{second}}$ is the input-referred noise of the first-stage and second-stage amplifiers, respectively, and $A_{OL,first}$ is the open-loop gain of the first-stage amplifier. The overall noise contribution from the second-stage could be neglected, because usually the open-loop gain of the first-stage $A_{OL,first}$ is large enough. Besides, the second-stage could be biased in much lower current than first-stage without degrading the overall noise performance. The equation (6) could be simplified to:

$$V_{ni,OPA}^2 = V_{ni,first}^2 \quad (7)$$

For the first-stage amplifier, the major noise sources are due to the differential-pair input transistors J_1 and J_2, the emitter-degeneration current sources, and the resistor R_1. With an appropriate choice of degeneration resistance of R_3 and R_4, the noise contribution from the emitter-degeneration current sources can be made mainly from the degeneration resistors. The input-referred noise of the first-stage can be approximated as:

$$V_{ni,first}^2 = [\frac{1}{g_{mj1}^2}(\frac{16kTg_{mj1}}{3} + \frac{8kT}{R_3}) + 4kTR_1] \cdot \Delta f \quad (8)$$

By observing equation (8), in order to minimize the input-referred noise of the first-stage, the transconductance of the input JFET (g_{mj1}) should be maximized at a given bias current level by choosing a large W/L ratio. However, in the meantime, we need to notice that a large W/L ratio would result in a large input capacitance. Thus, there is a trade-off to make the W/L ratio.

III. Simulation Results

Our proposed instrumentation amplifier was simulated based on 0.6 µm BiCMOS process with JFET module from a power supply of 2.8 V. From equation (3), the ratio of R_2 to R_1 was set to be 20, and the ratio of R_f to R_s was 5 to get a closed-loop gain of 40 dB. Our amplifier draws a total current of 3.65 µA, which can be broken down as follows. The first-stage consumes 3.13 µA (85.7%), the second-stage consumes 0.23 µA (6.3%), and the CMFB consumes 0.29 µA (8%).

The simulated transfer function of the amplifier is shown in Fig. 3. The mid-band gain of the instrumentation amplifier is 39.86 dB. The 3-dB corner frequency is around 7.4 kHz.

Fig. 4 shows the input-referred noise spectrum of the amplifier. Due to the use of JFETs as the input devices, the flicker noise corner is quite low, which is below 100 Hz. The input-referred thermal noise density is about 38 $nV/\sqrt{Hz}$. The total input-referred noise integrated from 10 mHz to 100 kHz is 3.81 μV_{rms}. To compare the power-noise tradeoff among amplifiers, the noise efficiency factor (NEF) reported in [9] is adopted:

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \quad (9)$$

where k is boltzmann constant, U_T is the thermal voltage, $V_{ni,rms}$ is the total input-referred noise of the instrumentation amplifier, I_{tot} is the total supply current, and BW is the -3 dB bandwidth of the amplifier. By using equation (9), our calculated NEF is 3.23.

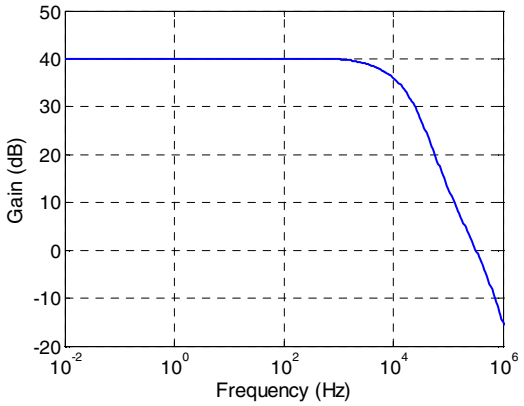

Fig. 3. The simulated transfer function of the instrumentation amplifier.

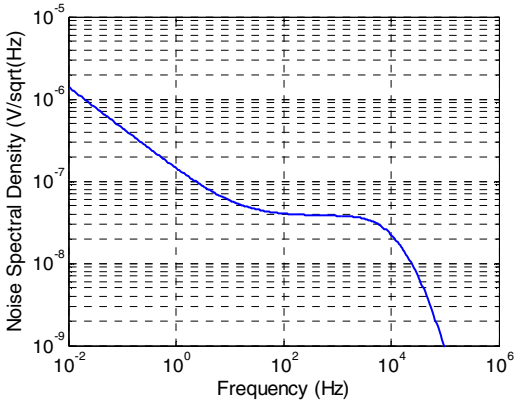

Fig. 4. The simulated input-referred noise spectrum of the amplifier.

Fig.5 shows the simulated common-mode rejection ratio (CMRR). The simulated CMRR is better than -100 dB in the bandwidth of interest. Fig.6 shows the simulated power supply rejection ratio (PSRR), which is lower than -80 dB in the bandwidth of interest.

The performance of our amplifier is compared with several other state-of-the-art instrumentation amplifiers in Table I.

TABLE I
INSTRUMENTATION AMPLIFIER PERFORMANCE COMPARISON

	[1]	[3]	[4]	[5]	[7]	This Work
Current (μA)	1	16	.872	12.1	230	3.65
Vdd (V)	1.8 to 3.3	+/-2.5	2.8	1	5	2.8
Input capacitance (pF)	/	20	20	>20	/	1.39
Input resistance (Ω)	8M	>> 10 M	>> 10 M	>> 10 M	/	15.3 G
Gain (dB)	41	39.5	39.4	40	/	39.9
BW (Hz)	180	7.2k	1.3k	10.5k	/	7.4k
$V_{ni,rms}$ (μV)	0.95	2.2	3.07	2.2	/	3.81
NEF	4.6	4	3.09	2.9	8.8	3.23
NEF^2.Vdd	38.1	80	26.7	8.4	387.2	29.2
CMRR (dB)	> 100	≥ 83	> 66	80	> 120	> 100
PSRR (dB)	/	≥ 85	> 80	≥ 80	> 120	> 80

Our amplifier achieves comparable NEF of 3.23, but exhibits much higher input impedance than the amplifiers reported in [1], [3], [4] and [5]. Because the conventional NEF does not consider the supply voltage, a modified metric NEF^2.Vdd [10] is included in Table I. Compared with the amplifier [3], our amplifier achieves much better modified NEF. Compared with the chopper-stabilized amplifier [7], our amplifier features a much better NEF, because the ripple reduction loop degraded the noise-power efficiency.

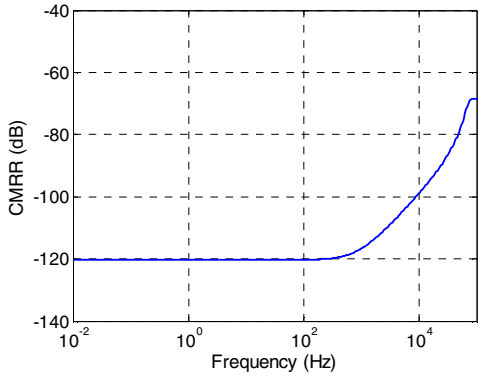

Fig. 5. The simulated CMRR of the instrumentation amplifier.

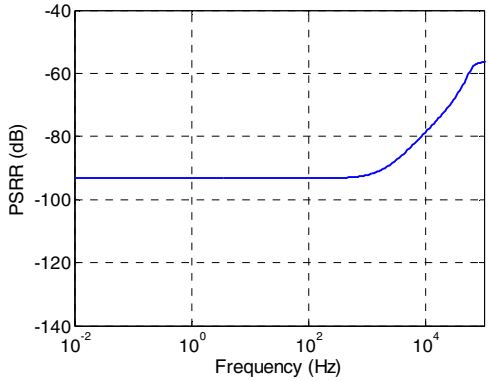

Fig. 6. The simulated PSRR of the instrumentation amplifier.

CONCLUSION

On the contrary to low input impedance, high input impedance instrumentation amplifier allows working with electrode interface having either high or low impedance. In this paper, our proposed amplifier exhibited high input impedance (15.3 GΩ||1.39 pF) by using JFET input and the additional feedback path through the sensing terminals. By utilizing several useful techniques, such as active cascode and emitter-degeneration current source loads, the noise-power efficiency was optimized. Our amplifier had input-referred noise of 3.81 μV_{rms} with a corresponding NEF of 3.23.

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