An Ultra-Low-Power 902-928MHz RF Receiver Front-End In CMOS 90nm Process

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***Abstract*—This paper presents a CMOS RF receiver front-end suitable for ultra-low-power operation. In order to achieve desired gain and linearity of receiver front-end at a 1V supply voltage, current reuse and optimum gate biasing techniques are employed. The proposed architecture includes merged LNA and mixer, operating in the sub-threshold region, and designed for the 902-928MHz ISM band. The proposed circuit is designed in a 90nm CMOS Process and occupies 0.04mm^2. The post-layout simulations of front end show a voltage gain of 17.8dB, a noise figure of 6.7 dB and IIP3 better than -8 dBm. Its power consumption is only 218uW from a 1V supply.**

***Index Terms* — CMOS, low-noise amplifier, mixer, front-end, low power, ISM**

I. Introduction

Implantable biomedical communication devices are now at the forefront of extensive research. These devices may effectively capture vital information from the outside environment for use as substitutes for human organs (i.e bionic ear, bionic eye, etc.), and/or record real-time physiological parameters from a patient (e.g EEG,ECG,EMG, blood pressure, etc.). Transceivers for these purposes require extremely low power consumption, since batteries are undesirable due to their limited lifetime and the possibility of infections, and hence power is preferably acquired by wireless coupling [1].

To date, most ultra-low-power sensor nodes have used simple architectures such as super-regenerative and sub-sampling receiver [2]-[3]. Although a sub-sampling receiver using passive high-Q resonators consumes very low power, they require rather expensive passive components, such as FBARs and RF-MEMS. For high data-rate and low cost, low power application, standard CMOS homodyne or super-heterodyne RF receivers are preferred.

In this paper, we present an ultra-low-power CMOS 902-928 MHz receiver RF front-end with the objective of minimizing power consumption while achieving the required performance. Section II briefly addresses the system level design. Section III describes the circuit design in detail. Section IV presents the simulation results followed by the conclusions in Section V.

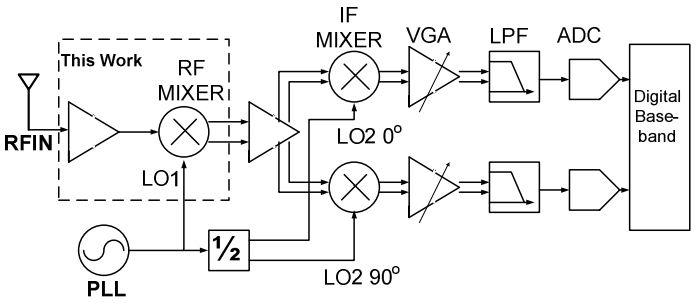

Fig 1. Block diagram of Receiver

II. System Level Design

The data rate is critical to the efficiency of the design. With a very high data rate the receiver consumes a large amount of power and bandwidth, whereas a low data rate requires the transceiver to stay on for longer duration transmitting the same amount of data. Specifications will vary with the specific applications, but the Zigbee standard provides an example of typical requirement for a low-power radio. A data rate of 40kbps, according to 915MHz ISM band Zigbee standard, is assumed to be sufficient for most application involving wireless data transfer. Based on a bit error rate (BER) of 10^{-4} and minimum sensitivity requirement (-92dBm), required specifications can be derived with OFSK modulation scheme [4-5], as shown in Table I.

TABLE I. SPECIFICATION OF 915MHz RF RECEIVER

Eb/No(dB)	12.2
SNR_{min}(dB)	9
NF_{max} (dB)	19.2
IIP3(dBm)	-33

Here, NF_{max}= 19.2dBm with 5dB margin from the minimum sensitivity requirement of IEEE 802.15.4 standard. Also,

with a 10 dB margin, the calculated IIP3 is -33 dBm with an interfering power of -59dBm.

III. Receiver Front-End Implementation

The proposed receiver front end is designed for use in a sliding-IF receiver architecture, as shown in Fig. 1 [6]. The desired RF signal is down-converted to baseband through two-step mixing. The frequency of the first LO is 2/3 of the RF frequency, i.e. 600MHz, which result in a sliding IF frequency at 1/3 of the RF frequency. By applying the first LO through a divide-by-2 circuit, the second LO quadrature signal are generated with exactly the same frequency as the IF frequency. With this frequency plan, the image frequency of the receiver is also located at 1/3 of the RF frequency. The image frequency is far from the RF frequency and can be easily rejected by the external antenna and input matching network. Also, the first LO is well out of the band, so the LO emission is suppressed by the selectivity of the external RF component. The general advantages of the sliding-IF architecture are mostly fixed DC offset compared to direct conversion, and use of a single frequency synthesizer to generate the RF and IF LO. Quadrature LO generation at 1/3 of the signal frequency is also advantageous. The baseband I and Q signals go into the digital baseband after amplification, channel-selecting and digitalization through the VGA, LPF and ADC.

A. LNA

To achieve ultra-low-power performance, we have designed a single-ended LNA with NMOS transistor (M1) biased in sub-threshold region (see Fig. 2). The aspect ratio of NMOS transistor is optimized to increase the gain of the amplifier. In particular, to minimize the NF of LNA, first, transistor M1 should have minimum channel length [7]; Second, a capacitor C_d is connected between the gate and source terminals of M1 to achieve optimized quality factor of input matching network [8]. An inductor L_g and programmable C_d act as two additional degrees of freedom for input matching optimization. A source degeneration inductor *Ls* also helps to achieve good input matching, and provides good linearity. C_p is a parasitic capacitor from the PCB trace.

Since the drain current has an exponential characteristic with gate-source voltage in sub-threshold, it leads to higher ratio of transconductance to I_{ds} (g_m/ I_{ds}) in sub-threshold than in the strong-inversion region, with correspondingly improved power efficiency. It is true that this ratio saturates when the device enters the deep weak inversion region [9]. Also, In sub-threshold region, the saturation voltage (V_{dsat}) of a device is no longer depend on the gate bias. In this CMOS 90nm process, the V_{dsat} is around 50mV (2*UT*), where U_T is thermal voltage in room temperature, which makes very low power supply possible. However, to ensure the device is in saturation, and to alleviate the effect of drain-source voltage (V_{ds}) to the drain current I_{ds}, V_{ds} should be configured large enough (*>4~5* U_T) in practical application.

Furthermore, current MOS transistor noise model (BSIM4) predicts that the input-referred noise in sub-threshold regime increases significantly with decreasing drain current [10]. Recent research [10] has shown that the minimum NF of sub-threshold transistor saturates as the current is reduced. Therefore, noise figure in this design does not degrade drastically when M1 is biased in sub-threshold region. Note that the channel noise of MOS transistor is frequency independent in strong-inversion region, however, as the device is pushed into sub-threshold region, frequency dependence is observed [8].Fortunately, channel noise power density is decreased as frequency decreases in sub-threshold region. Unlike the channel noise, induced gate noise is roughly proportional to square of frequency. In addition, the multiple finger and double gate connection MOS transistor in layout could lower the gate current thermal noise further [11].

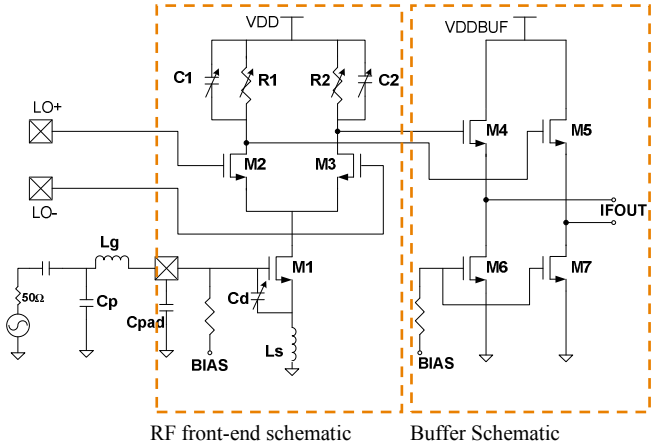

Fig 2. Schematic of proposed CMOS RF front end with RF input matching network.

Drain current of MOS transistor can be express in terms of gate-source voltage V_{gs} using the power-series expansion

$$i_d = g_1 v_{gs} + g_2 v^2_{gs} + g_3 v^3_{gs} + \cdots \qquad (1)$$

Where $\boldsymbol{g}_i$ *is* the *i*th –order derivative of the dc transfer characteristic of MOS transistor. The third-order nonlinearity of the LNA NMOS is a major source of IMD3, which determined IIP_3 performance of proposed circuit.

Optimum gate biasing can minimize the 3rd-order inter-modulation distortion (IMD) [12].Through the simulation, $\boldsymbol{g}_3$ =0 if gate was biased at 402.6mV. However, since the source degeneration inductor creates a feedback path for 2nd-harmonics of drain current, it will generate a negative term in IMD. Minimum IMD can be achieved if $\boldsymbol{g}_3$ is adjusted to positive value, which will cancel the negative term in IMD. That's why actual gate bias voltage in our design is slightly lower than that simulated value.

B. MIXER

A single-balanced mixer is chosen to share DC bias current with LNA. Here, transistor M1 was also treated as a transconductance stage for the mixer. A commutating differential pair mixer is resistively loaded for small chip size. Although the series load resistor requires valuable

voltage headroom, alternatives suffer from their own problems. For example, a differential load with active PMOS pull-up current source can operate with lower headroom, but suffers from large flicker noise. A programmable capacitor array is added to the mixer's load to act as a low pass filter to suppress the high frequency spurious noise.

The commutating differential pair of mixer is also biased in sub-threshold region, which can provide higher g_m at a given bias current. Therefore, switching slope of differential LO signal becomes steeper, which leads to more ideal square LO signal and accordingly higher conversion gain. Simultaneously, it can lower both mixer noise and nonlinearity [13].In addition, required LO signal swing for switching LO transistor to steer the small sub-threshold bias current can be made very small. As a result, requirement of LO signal power is expected to be relaxed in sub-threshold mixer design, which can lower the power for LO signal generation block.

The mixer's output connects to a source follower (M4-M5) with current source (M6-M7) for flexible testability, because the gate bias of current source can be controlled by an external voltage source.

IV. SIMULATION RESULT

The RF receiver front-end has been designed and laid out in 90nm CMOS technology and consumes only 218uA from 1.0V supply. Circuit level and post-layout simulations were performed in Cadence Spectre-RF following parasitic RC extractions with the aid of Calibre. During the simulation phase, off chip components are replaced by the real model provided by vendor. Also, the package model, bond wire model and PCB trace model are included in the simulation. As shown in Fig 3, input matching is good with input return loss less than -22dB across the ISM band (902MHz-928MHz). Post-layout simulations show that the proposed front end achieves a 17.8dB voltage conversion gain at an IF frequency of 305MHz, as shown in Fig 4. The variation of voltage gain is less 0.85dB across entire ISM band. Above simulation result is based on the fixed LO frequency with varied RF frequency.

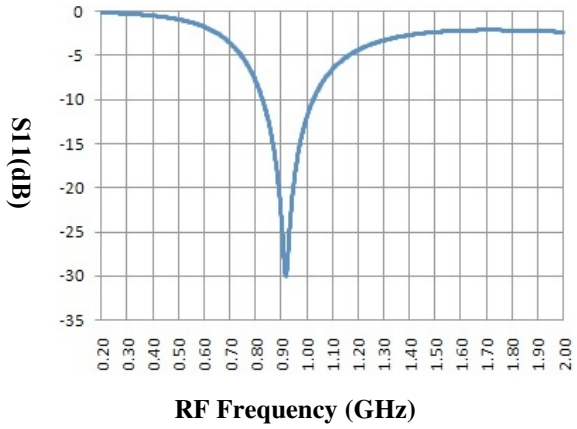

Fig 3. S11 simulation result of RF front-end.

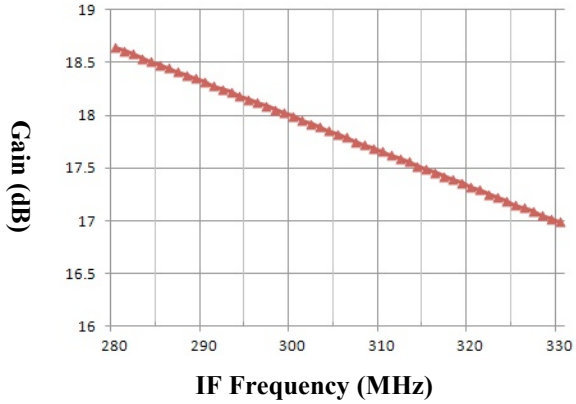

Fig 4. Gain of RF front-end. (17.8dB@305MHz)

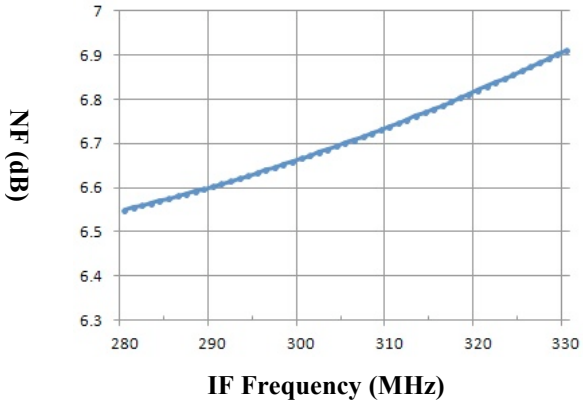

Fig 5. NF of RF front-end. (6.7dB@305MHz)

As shown in Fig 5, NF is 6.7dB at 305 MHz IF frequency. For a given quality factor (Q) of input matching network, minimum NF of LNA can be achieved if optimum width of transistor M1 and ratio of ($C_{gs}/C_d + C_{gs}$) are chosen appropriately [8]. In this design, the size of M1 is chosen to maximize gain at the expense of a slightly increased noise figure.

A two-tone test at 910MHz and 915MHz was performed to simulate the fundamental signal output power and third-order inter-modulation signal output power (IM3).The result of these simulations is plotted in Fig 6. The third-order intercept point (IIP3) is -7.5dBm. Gain compression point is -21.7dBm, as shown in Fig 7.

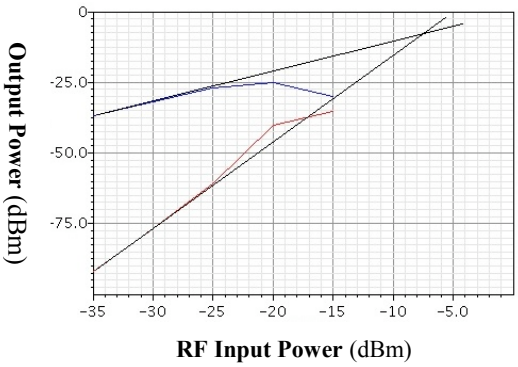

Fig 6. IIP3 plot of RF front-end

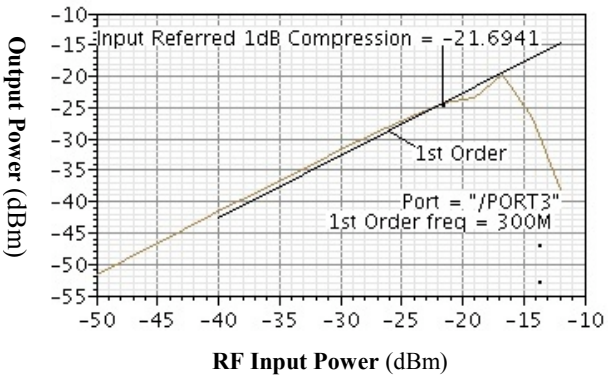

Fig 7. P1dB plot of RF front-end. (-21.7dBm)

Table II summarized the performances of the proposed front-end and other reported low power RF CMOS front-ends [14-17]. The overall performance of RF front-end can be expressed by a figure of merit (FOM).

$$\mathrm{FOM} = 20\log_{10}(f_{RF}) + CG - NF + \mathrm{IIP3} - 10\log_{10}(P_{DC})$$

According to the comparison result of Table II, the proposed RF front-end has best performance of similar published receiver front ends.

V. Conclusion

We have proposed an ultra-low-power CMOS receiver front-end for wireless sensor nodes operating at 902-928MHz ISM-band. System and circuit level design for a sliding-IF receiver have been presented together with the post-layout simulations. The proposed front end utilizes current reuse and optimum gate biasing technique, which achieves high performance suitable for low power wireless biomedical device application. The post-layout simulation results summarized in Table II demonstrate the RF front-end performance improvements over existing implementations.

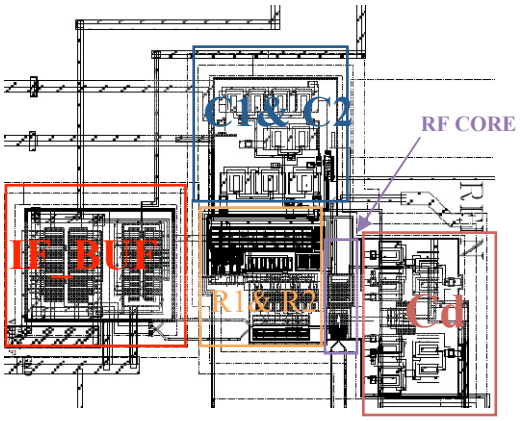

Fig 8. Layout of RF front-end.

TABLE II. LOW POWER RF FRONT-END PERFORMANCE COMPARISIONS

Metrix	[14]	[15]	[16]	[17]	This work
Process	90nm	130nm	180nm	180nm	90nm
Gain(dB)	16	32	30	30.5	17.8
NF (dB)	8	10	5	10.1	6.7
IIP3(dBm)	-14	-22	-37	-21*	-7.5
P1dB (dBm)	-23	-	-	-31	-22
VDD/IDD(mA)	0.5/3.2	1.2/0.77	1.2/0.87	1.2/4.5	1.0/0.22
Frequency(GHz)	2.4	0.915	2.5	2.4	0.915
F.O.M	209.56	209.57	205.77	218.79	219.4

*IIP3 is estimated from its P1dB

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