11.9 A 500µW Neural Tag with 2µV_{rms} AFE and Frequency-Multiplying MICS/ISM FSK Transmitter

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Advances in electronic-neural interfaces have shown great potential for both neuroscience research and medical devices. Much of the work to date has focused on short-range inductive links for power and communication transfer [1]. There is an emerging need for active miniaturized systems that stream neural data in the far field, which would enable the observation of brain activity in unconstrained animals such as mice or moths. Such systems cannot rely on near-field power transfer, and must be powered by small batteries or energy harvesters. We present a 500µW fully integrated neural interface that wirelessly streams a digitized neural waveform over 15m.

As shown in Fig. 11.9.1, the neural interface comprises an analog front-end with gain variable from 42 to 78dB, an 8b ADC, and a 100kb/s 2-FSK transmitter. The system operates in the Medical Implant Communications Service (MICS, 402 to 405MHz) and 433MHz ISM bands. A new transmitter architecture allows high power efficiency for low output power MICS-band communications. Also presented is a new complementary fully-differential low-noise analog front end with a Noise Efficiency Factor (NEF) of 2.48.

A programmable amplifier, shown in Fig. 11.9.2, amplifies microvolt-level signals over a 25mHz to 11.5kHz bandwidth. AC coupling at the inputs of both the LNA and VGA prevent offset amplification. A fully differential closed-loop architecture is used to ensure sufficient linearity and supply rejection. The LNA inputs are AC-coupled using 20pF capacitors and high-resistance (>100GΩ) MOS-bipolar pseudo-resistors. Separation of the signal and bias paths allows the input to simultaneously drive the n- and pFETs of the input stage. This complementary-input strategy doubles the effective transconductance for a given bias current while the output noise remains constant, thus reducing the input-referred noise voltage by a factor of two [2]. Thick-oxide MOS transistors with large gate areas are used at the input to reduce gate leakage while minimizing 1/f noise. The variable gain amplifier (VGA) consists of a complementary rail-to-rail folded-cascode core with programmable capacitive feedback. Six-level variable gain is set by selecting the feedback capacitors; the six variable high pass corners are set by programming the feedback transconductor bias current. Alternately, high impedance pseudoresistor feedback can be selected to obtain a sub-Hz high pass corner. The VGA is sampled by an 8b SAR ADC, designed to operate at sample rates from 10 to 100 kS/s.

The system streams one channel of continuous spike data sampled at 8b, 9.1kS/s with interleaved synchronization packet headers. We target a 100kb/s datarate and the maximum allowable MICS-band EIRP of -16dBm (25µW) to maximize communication range for untethered animal *in vivo* experimentation. Low power transmitters traditionally suffer from poor global efficiency since the frequency generation and modulation overhead begin to compete with the power amplifier dissipation. These effects are addressed by employing a new transmit architecture that operates entirely at the on-chip crystal reference frequency (44.545MHz) and drives a 9× frequency multiplying power amplifier, as shown in Fig. 11.9.3. The baseband FSK data directly modulates the reference oscillator using capacitor pulling. A 4pF on-chip capacitor creates a 16.4kHz $\Delta f_{ref,}$ resulting in approximately 148kHz FM frequency deviation at the 400MHz carrier.

The reference clock drives a 9-stage DLL. Each non-inverting delay stage in the DLL consists of a current-starved inverter controlled by two feedback loops for frequency and duty-cycle control, respectively. The operation of the edge-combiner (EC) is dependent on the overlap of rising and falling edges for a period of T/18, where T is the period of the reference input at 44.545MHz. Edge-combiner performance is critically dependent on equally-spaced edges from the delay cells of the DLL. Balancing delay-stage loads, symmetric layout, and dual-edge locking are essential for maximizing output power and minimizing reference spurs. This topology allows operation of the entire DLL at 44.545MHz, allowing quartz stability without the need for an RF carrier frequency PLL/DLL. This technique can be generalized to other multiplication factors, determined by the number of stages in the DLL and switching legs in the edge-combiner. Both DLL loops must demonstrate sufficient bandwidth to track the FSK baseband signal.

The edge-combiner behaves like a high-efficiency non-linear power amplifier, and produces pulses of current based on overlap of separate delay cells in the DLL. This current is absorbed by a tapped-capacitor LC matching network, which transforms the TX source impedance to match a 50Ω antenna and attenuates out-of-band spurs. The measured $|S_{22}|$ is shown in Fig. 11.9.3, showing better than -10dB return loss over a 30MHz bandwidth. This tank produces a sinusoidal voltage waveform of amplitude, $2/\pi I_{tail} R_p$ where R_p is the loaded tank impedance and I_{tail} is the edge-combiner DC current.

The proposed system was implemented in a 2.5×1mm² die, shown in Fig. 11.9.7, using a 0.13µm CMOS process. All biasing, logic, and passives are integrated on-chip except for two quartz resonators and 7 passive components, used for antenna impedance matching, DLL loop filtering, and system clock generation. The overall transfer function for the analog front end and the measured LNA input-referred voltage noise spectrum are shown in Fig. 11.9.4. The measured gain is adjustable between 42dB and 78dB. The integrated noise from 0.1Hz to 25.6kHz is 1.9µV_{rms}. The power dissipation of the entire analog front-end, including ADC and biasing, is 75µW.

The measured transmitter FSK deviation of 145 kHz is shown in Fig. 11.9.5. The quartz-based transmitter provides 2ppm frequency stability over the relevant 25 to 45°C MICS temperature specification, eliminating the need for frequency tracking algorithm as in [4]. The transmitter consumes 400µW with a -16dBm output power at a 100kb/s datarate with an edge combiner PA efficiency of 16%. The data rate for the transmitter is limited to approximately 200kb/s by the 1µs settling time of the DLL. The in-band measured spurs are less than -30dBc, conforming to the MICS standard. Reference spurs, offset from the carrier by multiples of f_{ref}, result from unequal delay in the delay cells due to random process mismatch and systematic layout related load imbalances. The measured reference spurs at 44.5MHz offset from the carrier are -22dBc, falling below -40dBc with a narrow-band antenna.

System functionality was verified by applying artificial neural spikes of 160µVpp amplitude at the input, and reconstructing the signal from digital data taken from a commercial FSK receiver board located at a distance of 15m from the transmitter, using a 1/4-wave 50Ω antenna pair. Fig. 11.9.6 shows the reconstructed signal overlaid on the original spike and also summarizes the performance of the neural streaming system.

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References:
[1] R.R. Harrison, et al., "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 123-133, Jan. 2007.
[2] J. Holleman and B. Otis, "A Sub-Microwatt Low-Noise Amplifier for Neural Recording," in *Proc. IEEE Engineering in Medicine and Biology Society Conference*, pp. 3930-3933, Aug. 2007.
[3] W. Wattanapanitch, M. Fee, R. Sarpeshkar, "An Energy-Efficient Micropower Neural Recording Amplifier," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, pp. 136-147, June 2007.
[4] J. L. Bohorquez, J. L. Dawson, A. P. Chandrakasan, "A 350µW CMOS MSK transmitter and 400µW OOK super-regenerative receiver for Medical Implant Communications," *IEEE Symposium on VLSI Circuits,* pp. 32-33, June 2008.

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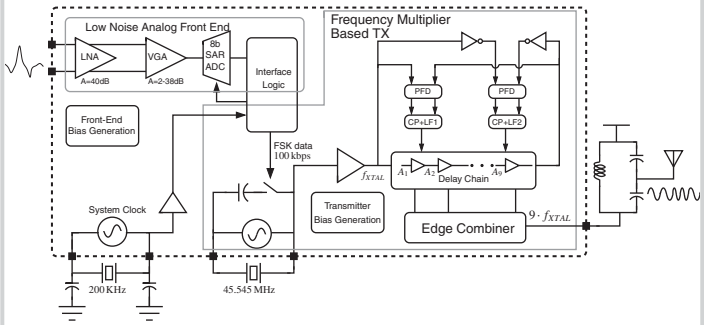


Figure 11.9.1: Neural spike streaming system block diagram.

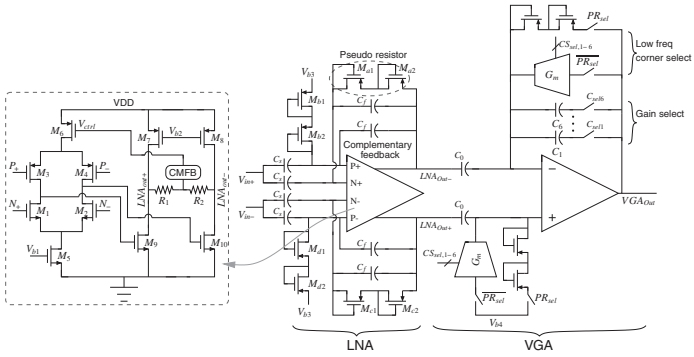


Figure 11.9.2: Low-noise analog front end schematic.

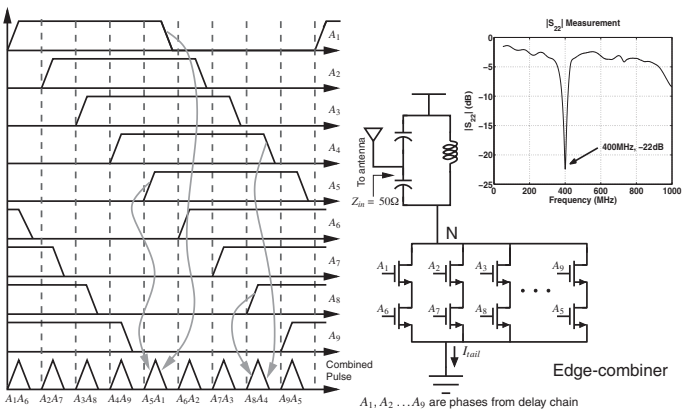


Figure 11.9.3: Transmitter edge combiner schematic details and measured output match, |S22|.

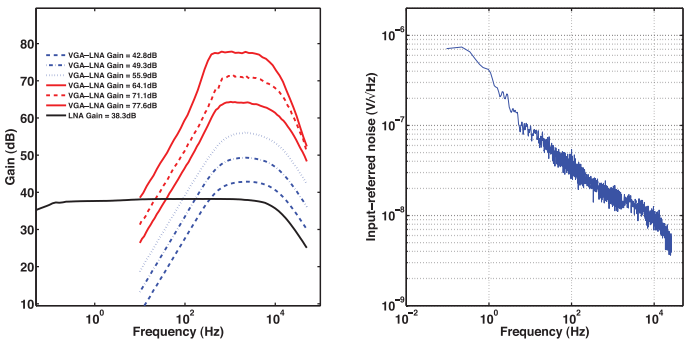


Figure 11.9.4: Measured gain and noise response of LNA and VGA.

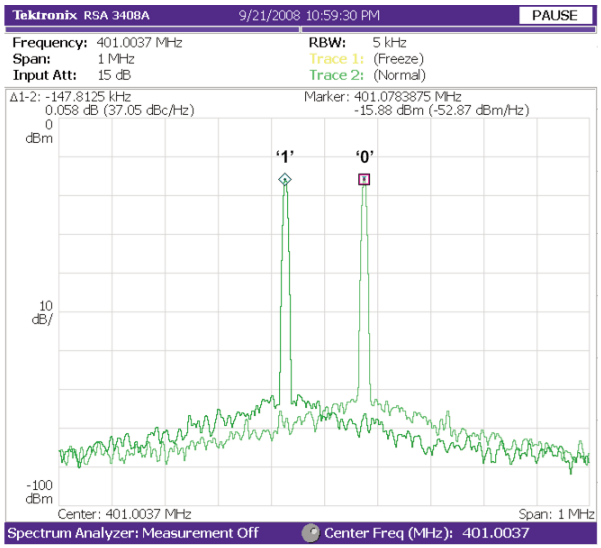
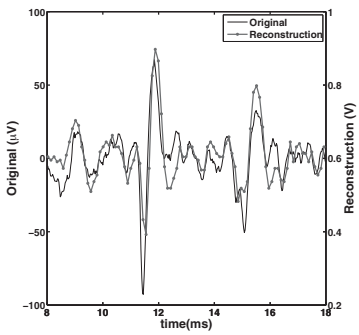


Figure 11.9.5: 401MHz Transmitter Spectrum, with FSK symbols overlaid.



Neural Tag Measurement Summary	
Tx Frequency Range (MHz)	300 – 450
Data rate (kb/s)	100
Modulation	FSK
PA Efficiency	~16%
CSR @ RF (dB)	In band > 30
XTAL start up time	< 1ms
DLL Locking Time	1μs
ADC ENOB	6.2
Power Consumption (μW)	
Tx Biasing + Ref. Oscillator	100
DLL	150
EC/PA	150
AFE	75
ADC	<1
Neural Tag Total	~500

LNA Measurement Summary & Comparison		
Parameter	This work	[3]
Supply Voltage (V)	1	2.8
Supply Current (μA)	12.5	2.7
Topology	fully-differential	single-ended
Gain (dB)	38.3	40.85
Bandwidth (Hz)	0.023 - 11.5k	45-5.32k
Input-referred noise (μVrms)	1.95 (0.1-25.6kHz)	3.06 (10Hz-98kHz)
Noise efficiency factor (NEF)	2.48	2.67
THD	1% (@1mV 130Hz input)	1% (@ 7.3mV 1.024kHz)
CMRR (dB)	> 63	66
PSRR (dB)	> 63	75

Figure 11.9.6: Reconstructed measured data and neural streaming system summary.

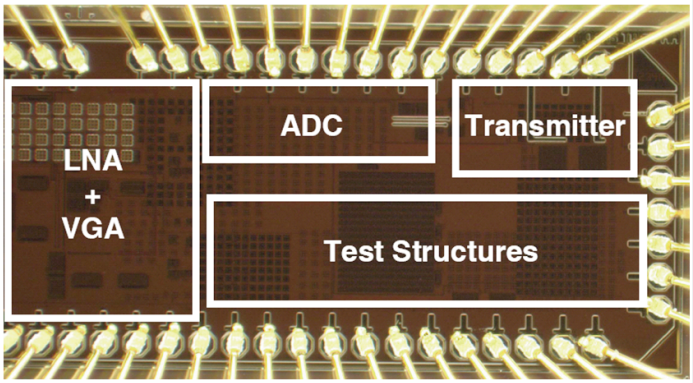


Figure 11.9.7: Chip micrograph of neural streaming system.

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