The Bumblebee: A 0.3 gram, 560μW, 0.1cm^3 Wireless Biosignal Interface with 10-m range

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ABSTRACT
The Bumblebee is a self-contained, ultra lightweight, low power 7.6 x 8.7 mm^2 wireless sensor capable of reliably transmitting data over 10 meters to a USB-compatible 433MHz receiver for approximately 3 days continuously on one 0.17g battery. With its small size, microvolt level noise floor, and 0.3g weight, the Bumblebee is well suited for on-body electromyography and other sensing applications where other wireless sensors are too costly, bulky, expensive, or simply unreliable.

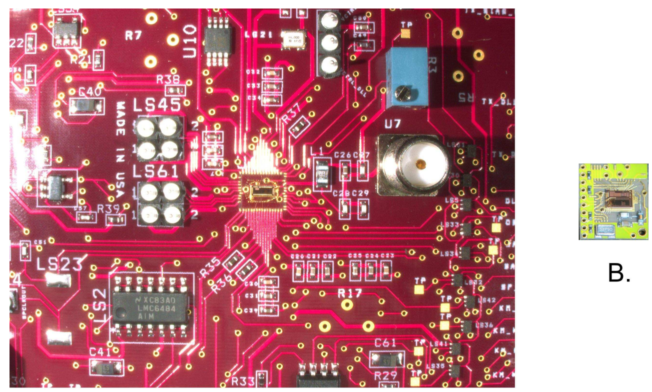
Categories and Subject Descriptors
B.4.1 [**Input/Output and Data Communications**]: Data Communications Devices

General Terms
Design, Human Factors

Keywords
Body area networks (BAN), neural recording, ultra-low power transceivers, low noise amplifiers

1. INTRODUCTION
The study of recorded biosignals is a very active area of research with many recent breakthrough systems developed to facilitate this task [1][5]. Wireless telemetry of these biosignals has enabled new discoveries into the foundations of neuroscience and brain computer interfaces [2]. The miniaturization of these systems will enable even more profound discoveries. In this paper, we present an ultra-low power, highly integrated system allowing robust amplification, digitization, and telemetry of microvolt-level electrophysiological signals. The 7.6mm x 8.7mm PCB contains a custom IC, all necessary passive components, and a 0.13 gram battery allowing over 17 hours of continuous recording and over 3 days of continuous recording when equipped with a 0.17 gram battery.

After a brief recap of the background of the Bumblebee, we discuss the architecture of the device and its custom receiver, implementation details, design strategy and tools, testing results, and finally conclude with some future applications of the Bumblebee.



A. B.

Figure 1. (A) 1st generation prototype chip and testboard. (B) 2nd generation chip on 0.1cm^3 thinned PCB.

2. BACKGROUND
The genesis for this work was our first-generation ultra-low power wireless neural interface chip presented in [3]. This chip contained two significant technological innovations that allow record-setting levels of power dissipation. First, the chip contained a complementary-input low noise biointerface amplifier allowing a noise efficiency factor of 2.5, the best reported for fully-differential amplifiers. Second, we verified a frequency-multiplying transmitter architecture that allows operation at a 1/9 fraction of the 400MHz carrier frequency. The printed circuit board (PCB) for this chip is shown in Figure 1(A). Although this chip exhibited very low levels of power dissipation, the testboard is far too large for on-body recording. Our goal for this project was a battery-powered system with a footprint less than 1cm x 1cm. To achieve this, we fabricated a 2nd generation chip allowing higher levels of integration and reduced power dissipation. Our completed system is 7.6mm x 8.7mm and is shown in Figure 1(B).

3. FUNCTIONAL DESCRIPTION
The Bumblebee is an ultra lightweight, high-performance, low power wireless sensor ideal for electromyography (EMG) and other sensing applications. It records a fully differential signal,

amplifies and digitizes the signal, and wirelessly transmits the data to a paired receiver.

Figure 2 shows the functional block diagram. The entire system is powered from a single 0.13 gram coin-cell battery, which is subsequently regulated to 1V. Other than this regulator IC [4], all functionality is performed by a single custom-designed IC. There is no non-volatile memory within this chip, so an external programmer is required to load appropriate settings for the chip (mode of operation, gain values, transmit power) upon powerup. The entire device is completely self-contained and compatible with a variety of recording paradigms (EMG, spike-based, audio).

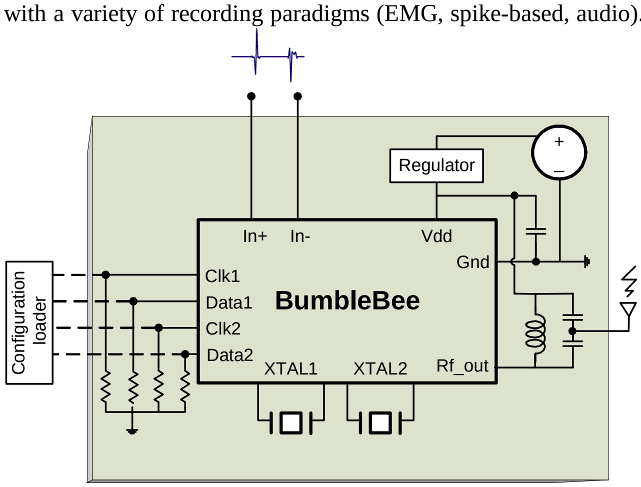


Figure 2. Bumblebee block diagram.

We developed a low-cost companion receiver for the Bumblebee. Since the receiver sits at a PC or basestation, it is not power-constrained and can utilize off-the-shelf electronics. This receiver reads in the wireless data transmitted from the Bumblebee, performs clock and data recovery, and reconstructs the analog signal as well as sends the digital sample data over a standard USB connection to a computer terminal for further processing. Figure 3 contains the block diagram of this receiver.

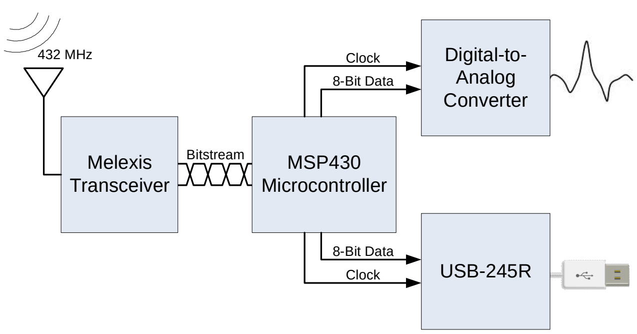


Figure 3. Companion receiver block diagram.

4. IMPLEMENTATION

4.1 Chip

For the Bumblebee system, we designed and fabricated a second generation custom designed 500µW fully integrated wireless bio-signal transmission interface chip which wirelessly streams a digitized bio-signal waveform over 15m, enabling further processing or actuation of a prosthetic device [3]. This system comprised an analog front-end with gain variable from 40-78dB, an 8-bit ADC, and a 100 kbps 2-FSK transmitter. We introduced a new transmitter architecture allowing high power efficiency for low output power MICS-band communications. The system operated in the Medical Implant Communications Service (MICS, 402-405MHz) and 433MHz ISM bands. We also presented a new complementary fully-differential low noise analog front end with a noise efficiency factor (NEF) of 2.48. This section briefly describes the enabling features of this chip.

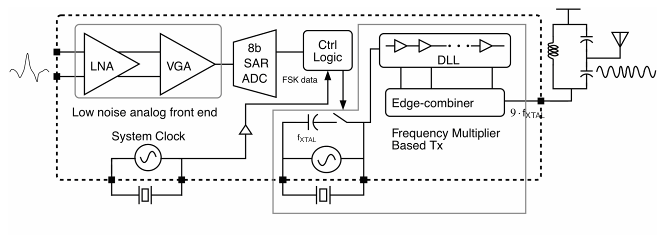


Figure 4. Block diagram of the integrated circuit.

4.1.1 Low Power Analog Front-End Circuitry

We have experimentally verified a biosignal amplifier that exhibits the best power-noise tradeoff (measured by the NEF) of closed-loop biosignal amplifiers reported to date (Figure 5). This circuit amplifies microvolt-level signals over a 25mHz to 11.5kHz bandwidth. AC coupling at the inputs of both the low noise amplifier (LNA) and variable gain amplifier (VGA) prevent offset amplification. A fully differential closed-loop architecture ensures sufficient linearity and supply rejection. Separation of the signal and bias paths allows the input to simultaneously drive the n-type and p-type transistors (nFETs and pFETs) of the input stage. This complementary-input strategy doubles the effective transconductance for a given bias current while the output noise remains constant, thus reducing the input-referred noise voltage by a factor of two. The measured gain is adjustable between 40dB and 78dB. The integrated input-referred noise is 1.9µVrms. The variable gain amplifier (VGA) consists of a complementary rail-to-rail folded-cascode core with programmable capacitive feedback. Six-level variable gain is set by selecting the feedback capacitors; the seven variable high pass corners are set by programming the transconductor bias current or selecting pseudoresistor feedback. The entire analog front-end consumes 28µW from a 1V supply (including bias).

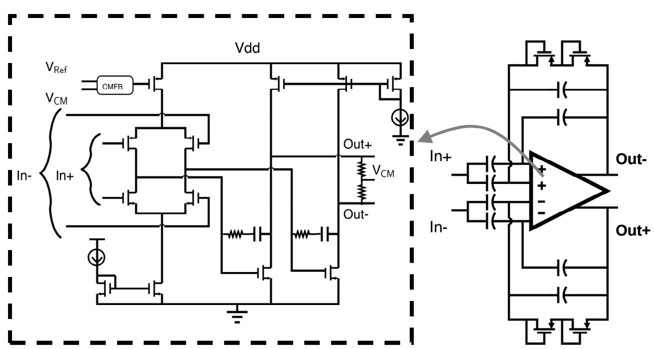


Figure 5. Fully-differential biosignal interface amplifier.

4.1.2 Low Power Transmitter Circuitry

For a reliable platform that can be given to biologists, neuroscientists, and healthcare professionals for deployment, the electronics must be robust and require a minimal amount of run-time calibration. Thus, the transmitter must utilize a true locked-to-quartz carrier frequency, unlike free-running LC oscillator-based transmitters that exhibit significant instability over supply, temperature, and antenna matching conditions. The challenge was to accomplish this with power dissipation much less than 1mW. In addition to power amplification, frequency synthesis and data modulation constitute a significant part of the total power budget of an RF transmitter. This results in poor global efficiency for low-power transmitters. Running the synthesis loop and modulation circuitry at a much lower frequency (F_{RF}/M) and multiplying it up by M at the power amplifier can allow transmitter operation at the on-chip crystal reference frequency. For our ISM band (433MHz) TX on the miniaturized Bumblebee board, we choose the reference frequency to be 48 MHz to drive a 9 frequency multiplying power amplifier, as shown in Figure 6 [3].

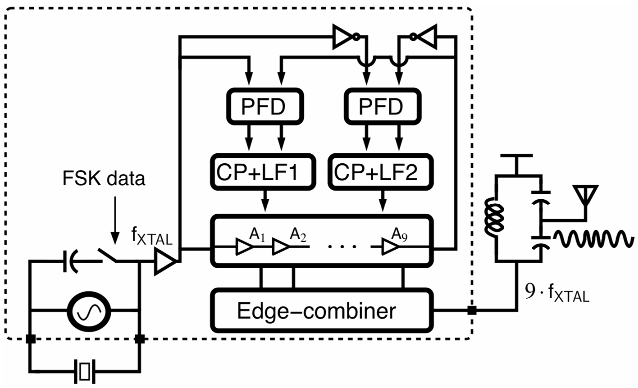


Figure 6. Architecture of the Frequency Multiplier-based ISM Transmitter.

The transmitter achieves very-low-power operation by replacing power hungry analog components like an RF phase-locked loop (PLL) with low frequency digital blocks like a delay-locked loop (DLL) and edge-combiner. CMOS scaling, voltage scaling, and frequency partitioning allow aggressive reductions in power consumption. The operation of the edge combiner (EC) is based on simple digital operations like AND, OR on the rising and falling edges derived from the delay chain of the DLL. Data modulation is accomplished by pulling the quartz reference clock. The resulting frequency deviation is also multiplied by 9X. Each delay stage in the DLL consists of a current-starved inverter. Since the operation of the edge combiner that multiplies the frequency critically depends on equally spaced edges, we employ dual-edge locking. The operation of the edge combiner (EC) is dependent on the overlap of rising and falling edges for a period of T/18, where T is the period of the reference input at 48MHz. The edge-combiner also behaves like a high-efficiency non-linear power amplifier, and produces current pulses of duration equal to T/18. The tapped-capacitor LC matching network transforms the TX source impedance to match antenna impedance and filters out the harmonics.

4.2 Power Supply

Power is provided to the device via a single coin-cell battery that is regulated down to 1.0V. A variety of watch and hearing-aid batteries are available in this size range (see Table 1).

Table 1. Energy/Size tradeoffs in commonly-available batteries

Battery	Chemistry	Voltage (V)	Weight (grams)	Capacity (mAh)
Energizer 337	Silver Oxide	1.55	0.13	8.3
Size 10	Zinc Air	1.4	0.32	91
Size 5	Zinc Air	1.4	0.17	33
CR1216	Lithium	3.0	0.6	34
Energizer 191	Manganese Dioxide	1.5	0.8	49
Energizer 164	Mercuric Oxide	1.4	0.36	24

A few observations are warranted. First, traditional sensor-network Zigbee-type radios that consume >20mW during transmission are unsuitable for this application due to their high peak and average power dissipation. Secondly, the energy density of low mass batteries is extremely limited and a sub-mW power dissipation is mandatory for a reasonable lifespan. All of the batteries evaluated experience significant voltage drop throughout the lifespan of the battery. Thus, voltage regulation for this system is very beneficial since it allows us to use batteries whose voltage changes during operation while at the same time provide an accurate voltage reference for the ADC operation of the chip.

The Seiko S-11L10 Super-Low Output Low Dropout CMOS Voltage Regulator [4] was chosen in conjunction with a 1µF bypass capacitor both because of its small size and low quiescent current, consuming only 9µA during operation.

Two different batteries were deemed suitable for the Bumblebee: the ZincAir Size 5 and the Silver Oxide 337. Each has a tradeoff between power density and total weight. ZincAir batteries have significantly higher energy density when compared to a standard Silver Oxide coin-cell, however commercially available sizes in this technology are larger than some Silver Oxide batteries.

For applications where the absolute minimum weight is needed, the Silver Oxide size 337 is ideal. It weighs only 0.13g and provides approximately 8.3mAh at 1.55V. When a slightly higher weight can be tolerated the ZincAir size 5 battery is the best choice. Weighing 0.17g, this battery provides 35mAh at 1.25V; a more than 3x increase in stored energy over the 337 battery for only 0.04g of additional weight.

4.3 Physical Size

The Bumblebee's functionality comes from a single chip, so the final product can be extremely small since minimal support circuitry is required. The Bumblebee uses a thin 4-layer PCB measuring only 7.6 x 8.7 mm^2. Low weight is critical to allow in-vivo experimentation on small animals (mice, rats) and insects (locusts, moths). The fully-populated PCB weighs 0.18g without battery, 0.3g with a 337 battery, and 0.34g with a size 5 zinc-air battery. Figure 7 shows the front and back of the Bumblebee with the unencapsulated chip mounted with chip-on-board (COB) connections. The deployed board used epoxy encapsulation to protect the bondwires.

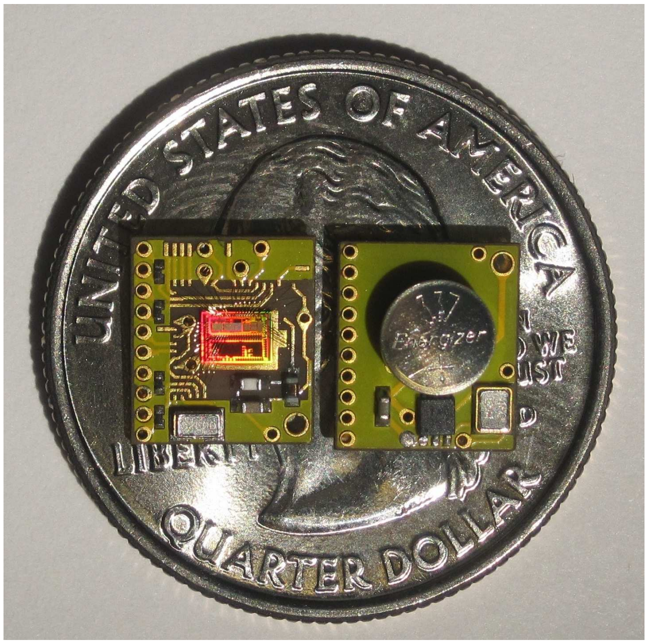


Figure 7. Front and back of the Bumblebee board. A thin 30 gauge wire-wrap monopole wire antenna a few cm long allows >10m range.

4.4 Receiver

An inexpensive receiver system was designed to collect the data transmitted from the Bumblebee. The block diagram for this receiver is shown in Figure 3. This receiver demodulates the signal, decodes the packet and outputs the raw data both via USB to a computer system as well as a reconstructed analog signal.

Demodulation occurs within the Melexis EVB7122 receiver. The resulting bitstream is processed by a TI MSP430F2012 microcontroller which runs a custom clock and data recovery (CDR) algorithm. The programming of the microcontroller was done in 'C' and is entirely interrupt driven to achieve accurate timing and avoid any operating system overhead.

Our CDR takes advantage of the fact that there is a built-in transition within each packet header of our transmitter to sync its timing reference, making the receiver quite tolerant to variances between the Tx and Rx clocks. An extreme example of clock mismatch is shown below in Figure 8. Here we see that the microcontroller waits a given amount of time according to its internal clock to sample the bitstream and determine the value of each bit. If this clock reference does not match perfectly with the clock used by the transmitter, the sampling train of the microcontroller will appear to drift away from the center of each bit, eventually resulting in either skipping a bit entirely or reading a single bit twice. To avoid this potential problem the microcontroller re-syncs its sampling train during the 0-1 transition contained in each packet's 011 header pattern by scheduling the next sample to take place one half of a bit period after this transition (instead of a full bit period after the previous sample as is done every other time). Theoretically, this method can tolerate as much as a 4.5% mismatch in clocks (maximum drift of ±50% of a bit period over eleven total bits per packet).

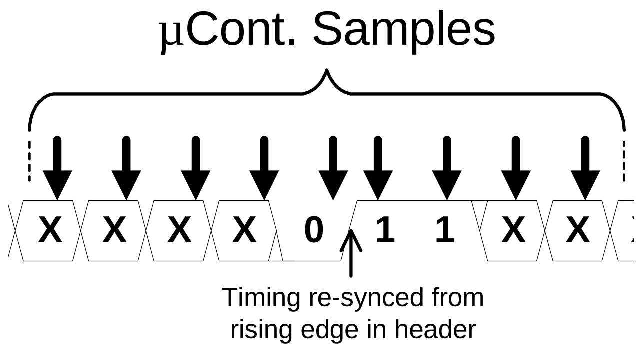


Figure 8. Rx timing synchronization with frequency mismatch.

The final extracted data is then sent digitally via USB (using FTDI's FT245R chip) to a PC as well as reconstructed as an analog signal using the TI TLC7524 8-bit digital-to-analog converter. This CDR algorithm is run on-the-fly, allowing realtime reconstruction of the analog waveform for viewing on a scope or for audio playback. The entire receiver system is powered from the 5 V bus provided by the USB connection.

The dual outputs of both analog and digital data allow for easy integration into legacy experimental setups where, for example, a biology lab uses analog visualization and audio playback equipment. At the same time, the USB interface provides pure digital samples for future digital signal processing (DSP) analysis and archiving.

The receiver itself is capable of processing data up to 300kbps. We are currently operating at 32.8kbps to allow a tiny watch crystal on the Bumblebee board. However, the relaxed frequency tolerance specs as described above will allow the use of microscale MEMS resonators for frequency definition, which is work in progress.

5. DESIGN PROCESS

The schematic for Bumblebee was developed using OrCAD Capture and PCB design was accomplished using OrCAD Layout. The schematic for this device is quite simple since it only contains a few components besides the custom IC.

A major goal of this design was to minimize the size of the final device, which required a sophisticated PCB layout. OrCAD Layout allowed us to fully define the specifications of our board (trace width, spacing, custom landing pads, etc.) so we could maximize surface density and minimize the final board size and ensure the board would be manufacturable.

The receiver microcontroller CDR code was written and compiled using IAR Embedded Workbench and the debug features within this program were used to validate the code.

The extremely small size of the board limited the accessibility of test points to assist in debugging. To minimize the need for post-fabrication debugging, a prototype of the entire system was built using a macro-scale test board similar to that shown in Figure 1(a). The prototype also confirmed the compatibility of the Bumblebee system with very small batteries.

quick succession.

A zoomed in view of a reconstructed EMG signal received from the Bumblebee (green) is shown in Figure 8 (C) overlaid on the original amplified EMG signal (yellow). This plot demonstrates the real-time clock and data recovery of the baseband and the low latency of the signal reconstruction

6. TESTING AND RESULTS

The Bumblebee board powered up and measured with a spectrum analyzer to view signal strength and verify operation. Initial testing was then performed to confirm the functionality and range of wireless transmission of our signal. A 10mV peak-to-peak sine wave was generated as a test input for the Bumblebee biosignal amplifier. Figure 9 (A) shows the reconstructed waveform from the receiver (top) along with the input signal to the Bumblebee (bottom). The transmitter was approximately 1 meter away from the receiver for this test.

Our initial deployment of the board is as a low power, unobtrusive EMG sensor. Differential EMG probes were used to apply a signal to the Bumblebee. The probes were attached to a forearm to measure muscle activity. The signal was transmitted over 10 meters to our USB-compatible receiver. Figure 8 (B) shows the reconstructed waveform resulting from three arm movements in

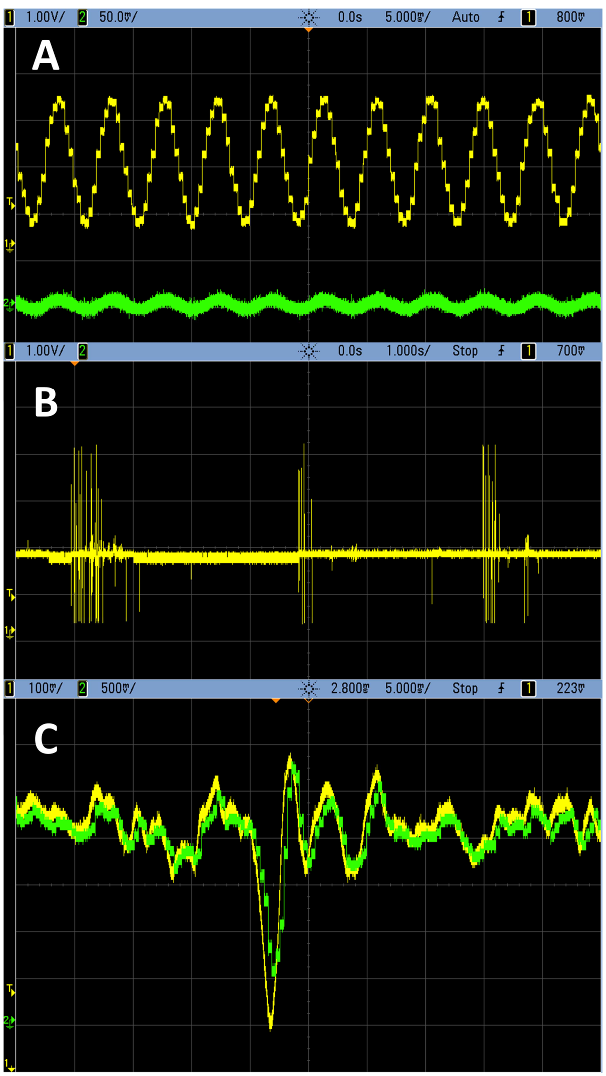


Figure 9. (A) A 10mV input signal (bottom) is amplified by the Bumblebee, digitized, transmitted, and reconstructed in real-time (top). The sampling points are clearly visible in the top waveform (B) Reconstructed EMG signal. (C) Zoomed-in EMG original and reconstructed.

The board power dissipation is 560μW from the nominally 1.2V ZA5 battery, while using the 1.55V 337 battery the Bumblebee consumes approximately 700μW.

Operational lifetime of the device is also dependent upon which battery is used. Battery and power supply traces from both the ZA5 and 337 batteries were recorded to determine continuous Bumblebee runtime. The results are shown in Figure 10. When powered by a Silver Oxide size 337 battery, the device continuously operates for approximately 17 hours before dying. When powered with a Zinc Air size 5 battery the Bumblebee will transmit for over 70 hours before the battery's energy is exhausted.

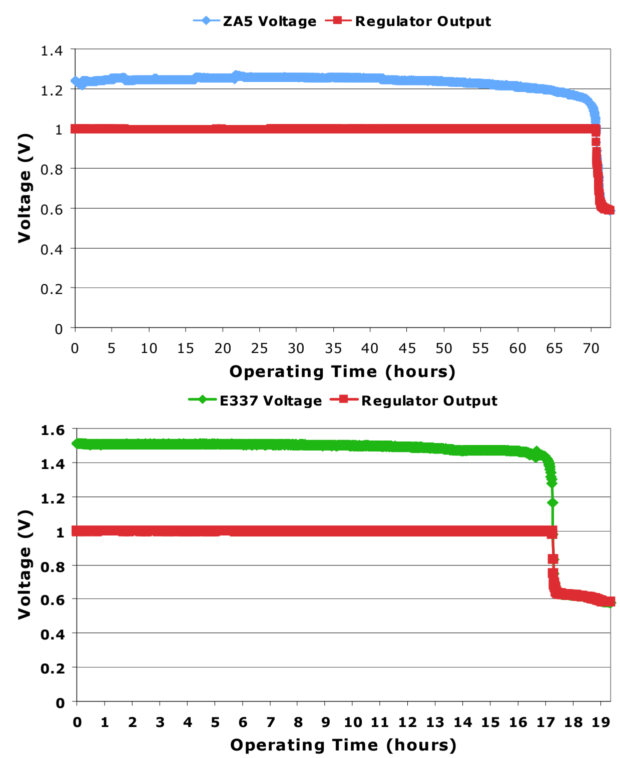


Figure 10. Operational lifetime using ZA5 (top) and 337 (bottom) batteries.

7. FUTURE WORK

There is a significant opportunity for extending this work both on the deployment side and on the technology development side.

7.1 Deployment

The small size and low noise floor open the door to a host of applications. Bumblebee devices will be provided to our collaborators to study brain and muscle signals of monkeys, perform temperature and muscle measurements on moths, and record brain signals on mice. In addition to electrophysiological recording, the devices can be used as a general-purpose wireless sensor platform. For example, we plan to investigate using the Bumblebee platform in conjunction with a MEMS carbon monoxide sensor to allow an inexpensive tiny CO detector used in many emergency response applications.

7.2 Technology

The main area for technological improvement is on the power supply side. We will experiment with powering the bumblebee from various energy sources (thermoelectric, solar, wirelessly-transmitted power). The low peak and average power dissipation open up new opportunities for energy harvesting beyond traditional wireless sensor network nodes.

By replacing the 32 kHz crystal used here with a higher-frequency resonator, the sampling rate could be increased, expanding the range of applications to those involving higher frequency signals, such as extracellular neural recording. Custom quartz crystals or MEMS resonators would provide suitable size and frequency.

The Bumblebee was designed to achieve the smallest possible size and weight. The flexibility of the Bumblebee could be improved with a moderate increase in size with the addition of a 1V flash-based microcontroller. Configuration data could be stored in the microcontroller's non-volatile memory, and could even be changed dynamically in response to recorded data. Because the majority of the circuits within the custom chip can be disabled through the configuration data, a microcontroller-based Bumblebee2 could periodically sample and transmit based on an interrupt-driven schedule, further extending the battery life for very low-frequency signals. Alternatively, a microcontroller could be used to perform rudimentary local processing and selectively transmit data based on its salience, effectively trading processing power for communication power.

8. CONCLUSION

In this paper we demonstrated a small self-contained, ultra lightweight, low power wireless sensor node built using the newly developed 2^{nd} generation wireless sensing chip. With this new chip we were able to drastically reduce the size and weight of the sensor and also reduce the number of required external components. The Bumblebee is capable of reliably transmitting data over 10 meters to a custom receiver, also described in this work, which can interface with applications requiring either digital or analog signals. Many different batteries were considered to power the device and ultimately two different commercially available ones were chosen, the 337 when the absolute lightest weight sensor is needed, and the ZA5 when both very light weight and long lifetime are desired. With its small size and 0.3g weight, the Bumblebee is the ideal solution for on-body electromyography and other sensing applications where other sensors are too bulky.

9. ACKNOWLEDGMENTS

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