A Low-Power Dynamic Comparator with Time-Domain Bulk-Driven Offset Cancellation

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***Abstract*—This paper presents a low-power dynamic comparator utilizing a novel time-domain bulk-driven offset cancellation scheme with minimal additional power consumption and delay. It uses an open loop dynamic phase detector to achieve very high precision. The circuit is designed in a 0.6-μm process. The simulation results show that the circuit consumes 540 nA current at 100 kHz clock frequency and the proposed offset cancellation scheme is able to reduce the input referred offset to within 25 μV from an initial value of 20 mV.**

I. INTRODUCTION

The comparator is an important circuit building block in data converter systems. In applications such as implantable devices, the use of low-power comparators in analog to digital converters (ADCs) is crucial because the heat dissipated by the device must not affect the surrounding tissue. In other energy-limited applications like wireless sensor networks, wearable instruments or portable devices, low-power is necessary to reduce the battery requirements and enable autonomous operation. Thanks to technology scaling down and newly proposed topologies, the power consumption of the digital parts in ADCs is continuously decreasing. However, the power consumed by the comparator does not decrease in proportion, making it the dominant power consumer in the system [1]. From the power breaking-down in [1], it can be observed that the analog power (most of which is consumed by the comparator) dominates the others, especially at lower clock frequency. To further decrease the power consumption, a dynamic comparator which does not consume static power is a more favorable solution.

A dynamic comparator utilizes positive feedback to achieve low power, high speed, high gain and full-swing output. However, it has a larger input referred offset compared to linear amplifiers. The reason is that in addition to static V_{th} and β mismatch, it also suffers from dynamic offset due to imbalance of parasitic capacitors at internal nodes during evaluation. This drawback will impact the resolution and yield of low power, high performance data converter systems.

A common way to reduce the offset is to use linear amplifiers and cancel the offset by negative feedback in auto-zeroing phase [2]. This scheme, however, requires unity gain stable amplifiers with considerable gain. Therefore, the advantage of no static power consumption is lost; and it will incur the trade-off between speed and power consumption. Recent publications have proposed other ways to cancel the offset of comparators. The comparator in [3] uses a pair of tunable capacitor arrays as the load of latch to adjust the offset, but this requires additional digital control circuitry to search for the proper capacitor values. Additionally, the capacitor loads will slow down the comparator. In [4], the authors propose a way to adjust the offset using imbalance of charge injection at latch nodes. Again additional circuitry is needed since the design itself cannot sense the offset. In [5] the latch can be reconfigured into an amplifier in the auto-zeroing phase thus implementing negative feedback; however it consumes static power in auto-zeroing phase and requires a complex timing control scheme and numerous switches. A novel time-domain comparator is presented in [6]. By cascading multiple delay lines, the design trades delay with input-referred noise and offset.

In this paper, we propose a novel comparator and offset cancellation (OC) scheme which is able to sense the offset in the time domain and eliminate it in closed loop. It does not significantly add to power consumption, sacrifice speed, or require complex timing control.

II. COMPARATOR DESIGN

A. Two Stage Dynamic Comparator

The simplified schematic of the core comparator is shown in Fig. 1. The design is inspired by [7]. However, several changes are adopted.

Firstly, the second stage is asynchronously clocked by the input signal. This will eliminate the need for a complementary clock and therefore save energy. Furthermore, the resolution is improved by input dependent regenerative feedback.

Secondly, the input transistors are changed from N type to P type. It is found that PFETs have a better flicker noise performance in this process, and the accessibility of the N-well body terminal makes the OC scheme possible.

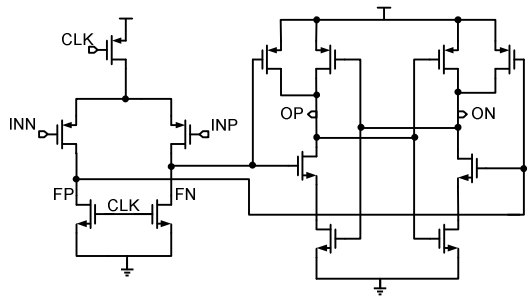

Figure 1. Simplified schematic of the comparator

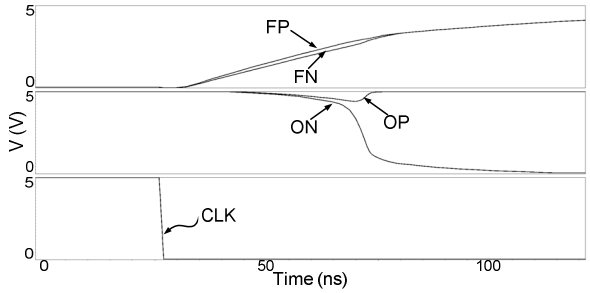

Figure 2. Typical waveforms of comparator operation

B. Operation

The operation of this comparator can be described as follows: when clock signal is high, nodes *FP*, *FN* are precharged to low and *OP*, *ON* high. A falling edge of clock signal stops the precharging phase and turns on the tail transistor of the first stage; both *FP* and *FN* rise but at different slopes because of the differential input *INP, INN*. When the common mode voltage of *FP* and *FN* reaches the threshold of the NFETs in the second stage, the amplification of the second stage takes over and *OP* & *ON* start to fall; finally the latch kicks in when the common mode voltage of *OP* & *ON* reaches the threshold of the cross-coupled inverter, the positive feedback regenerates the output to a rail-rail signal. This process is illustrated by Fig. 2. Here a 10 mV differential signal (*INP* > *INN*) is applied.

C. Two Stages Design

The first stage can improve the comparator's sensitivity and attenuate the input referred noise and offset of the decision stage. Therefore a large voltage gain is desirable. During comparison, the voltage gain of the first stage is approximately the intrinsic gain of the input pair.

$$A_{v_{intrinsic}} = -g_m r_o = -\frac{\sqrt{2\beta}}{\sqrt{I_D}\cdot\lambda} \quad (1)$$

From (1), we can increase the gain by reducing the aspect ratio of tail transistor to bias the input pair in sub-threshold. In this design, the gain of the first stage is about 30 when the decision is made. Therefore, the noise power of the second stage is attenuated by 900 times and the offset by 30 times.

III. Offset Cancellation Scheme

A. Principles and Architecture

The proposed OC scheme senses the comparator offset by measuring the delay between the two outputs and cancels it by tuning the body voltages of the input pair transistors. The system block diagram is shown in Fig. 3 above.

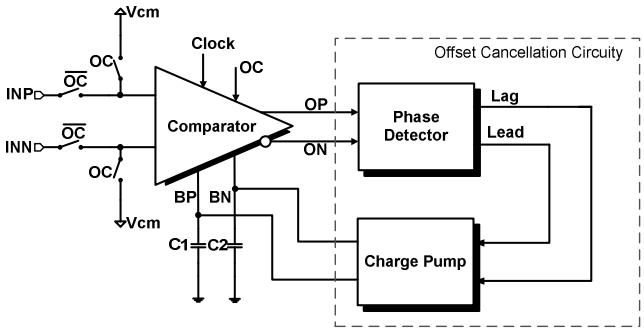

Figure 3. System architecture

In the ideal case in which all the transistors are matched, when the two inputs are shorted together, the voltages of *OP* and *ON* in Fig. 1 will fall at an identical rate at the falling edge of clock, whereas in the presence of offset, they will not. Therefore, the input referred offset can be represented by the delay between the two complementary outputs when there is no differential input. A phase detector (PD) detects the polarity and magnitude of the delay and drives a charge pump (CP). The charge pump changes the body voltage of the comparator input pair transistors. According to the body effect equation:

$$V_{TH} = V_{T0} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right), \quad (2)$$

the change of the input transistors' threshold voltage due to the body effect will be used to cancel the input referred offset.

B. Offset Cancellation Scheme

During the offset cancellation phase, comparator inputs are shorted to an appropriate common mode voltage and positive feedback is disabled so that delay can be obtained, C1 and C2 (the capacitors connected to the body terminals of the comparator input pair) are precharged to *Vdd*.

When clock is high, *OP* and *ON* are precharged to high. At the falling edge of the clock signal, the outputs start to fall. The delay between the two outputs due to input referred offset is sensed by the PD, which will generate pulses based on the polarity and magnitude of the delay. These pulses are sent to the CP and a certain amount of charge on C1 or C2 will be removed so that the body voltage change cancels the input referred offset.

Fig. 4 shows a typical waveform during OC. In this case, due to the offset, the falling edge of *OP* lags *ON*; the phase detector will sense this difference and generate pulses on Lag pin; these pulses will turn on the charge pump and as a result, the body voltage of one input transistor (*BP*) is decreased by ΔV while the other (*BN*) remains constant. If *OP* leads *ON* due to opposite polarity of offset, *BN* will be decreased in a similar manner (with *BP* unchanged).

There are several points worth noting about this scheme:

During OC, the comparator is operating in a way very similar to normal operation. Minimal number of components

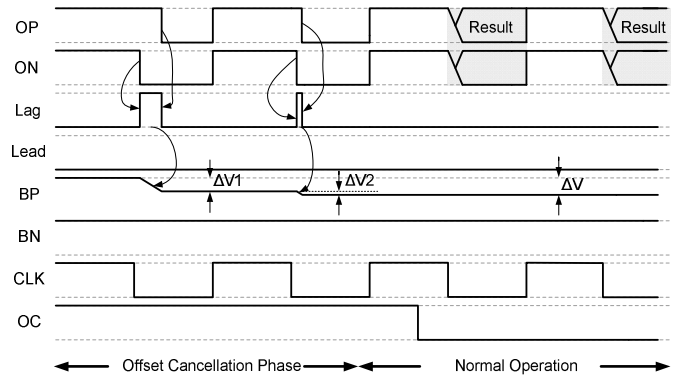

Figure 4. Typical waveforms during offset cancellation

are added to the comparator core to assist this process. In other words, the comparator is self-calibrating. And the offset is sampled at the output of comparator. Therefore this scheme is able to cancel the offset with high accuracy.

The OC action can be repeated multiple times (two times in Fig. 4). Each time the offset will be reduced to a fraction of its previous value. The amount of charge removed from C1 or C2 is proportional to the delay between the two outputs, hence the magnitude of input referred offset. The negative feedback nature makes this scheme converge fast and 98% of the offset can be eliminated in less than 3 iterations. It is observed that an extreme value of 100 mV offset can be reduced to within 100 μV in 3 clock phases.

The change of body voltage needed to cancel the offset depends on the magnitude of offset and γ in (2). In the worst case, it will not exceed 70 mV, so the input common mode range of the comparator will not be impacted.

C. Comparator Core for Offset Cancellation Scheme

To accommodate for OC, the comparator core is modified as indicated in the shaded areas in Fig. 5. Switches S1-S4 are added to disable the latch during OC. And the body terminals of the two input transistors are made accessible as *BP* and *BN*.

During OC, S3 and S4 are closed; S1 and S2 are open so that the latch is disabled. And the other transistors all operate just as in normal operation.

In normal operation, S3 and S4 are open; S1 and S2 are closed. The latch is enabled.

D. The Phase Detector

The function of the PD is to sense the delay between its two inputs. Conventional PDs based on latches or flip-flops as in [8] are not adequate in this application, because most of them suffer from a dead-zone issue, which will cause large residual offset after OC. Moreover, since they operate in closed loop, the speed is limited and the output jitter due to metastability [8] will add to random input-referred offset.

A simple and novel dynamic PD circuit is proposed to meet the requirements of the OC scheme. The schematic and timing diagram is shown in Fig. 6. The PD is enabled by *EN* signal and the output from the comparator is buffered with two

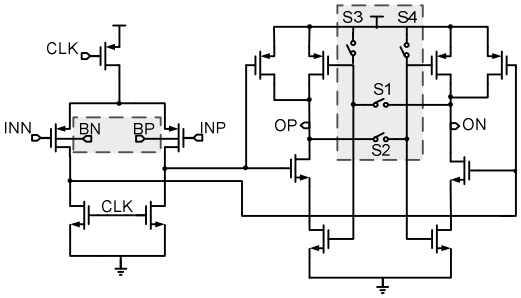

Figure 5. Modified schematic of the comparator core

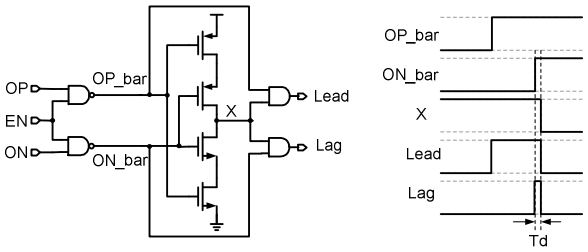

Figure 6. Shematic and timing diagram of the PD

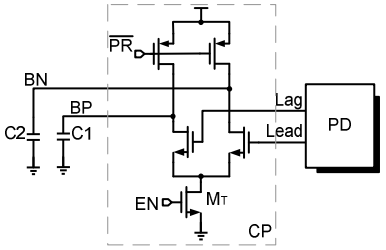

Figure 7. Shematic of the charge pump

NAND gates. The inverted signals *OP_bar* and *ON_bar* are then sent to a tri-state inverter. Note that the storage node X will not change its state unless both *OP_bar* and *ON_bar* change state. Therefore, the voltage at *X* is the inversion of the signal that comes later. The two AND gates will then generate pulses corresponding to the polarity and magnitude of delay. Especially, if the tri-state inverter has a small delay *Td* as shown in Fig. 6, pulses will be generated on both *Lead* and *Lag* wires, and the difference of pulse widths equals the magnitude of delay between the input signals. This effectively eliminates the dead zone.

The simple structure of the proposed PD makes it very power and area efficient. Open loop operation largely improves the speed and jitter performance. Simulation shows that the proposed PD is able to distinguish a 2.8 ps phase difference, corresponding to 5 μV input referred offset.

E. The Charge Pump

The charge pump is implemented as in Fig. 7, shown together with the PD and the capacitors connected to the bodies of comparator input pair (C1 and C2).

Before the OC starts, C1 and C2 are precharged to *Vdd* by a *PR* pulse. Then the CP is enabled by the *EN* signal, the two transistors connected to the PD will discharge C1 or C2 with pulse width controlled by the offset. The discharging current is limited by the tail transistor M_T.

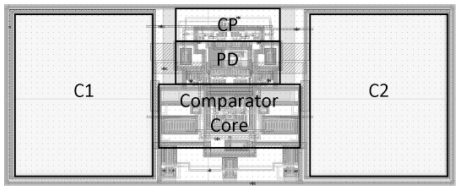

Figure 8. Layout of the comparator and OC circuitry

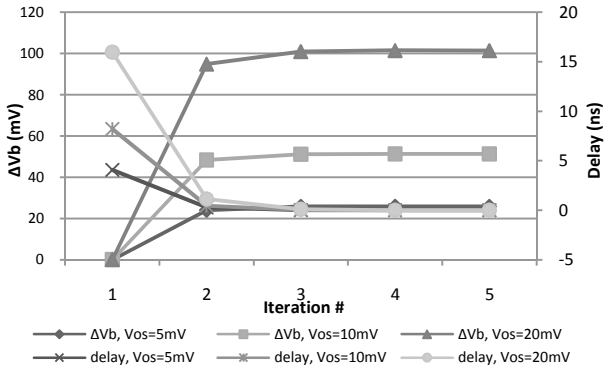

Figure 9. Convergence of offset cancellation

IV. Simulation Results

The proposed comparator with OC is designed in a 0.6-µm process and the layout is shown in Fig. 8. The performances based on post-layout simulation are listed in Table. 1.

To verify the effectiveness of the proposed OC scheme, a voltage source is added at one input of the comparator to simulate the input referred offset. The OC is executed for 5 iterations. The voltage difference between *BP* and *BN* (*ΔV*), and the delay between the *OP* and *ON* (*delay*) are plotted in Fig. 9. With initial offsets of 5, 10 and 20 mV, the circuit is able to converge in less than 3 iterations. After OC, the delay is reduced below 5 ps, and residual offset is less than 25 µV.

Furthermore, a statistical analysis is performed to determine realistic improvement on offset performance over process variation and device mismatch, accounting for offsets in sub-circuits such as PD and CP. One hundred iterations of Monte-Carlo simulation are performed with and without OC. The standard deviation of comparator offset without OC is 3.35 mV; with OC, it is reduced to 53.37 µV, indicating a 62.8 times improvement even with worst case process variation.

Since the time constant of voltages held in C1/C2 associated with leakage is on the order of 100 ms, frequent re-calibrating is not needed.

The system consumes dynamic current only and the OC circuitry can be disabled and does not draw any current in normal operation. It is worth noting that since the system operates in time domain; its performance will actually improve with technology scaling down, whereas the conventional approaches relying on precision analog processing will face serious performance degradation due to severe non-idealities of deep-sub-micron process. While the results above are obtained based on a 0.6-µm process, we expect that the performance (power, speed, precision, area etc.) will improve further at more advanced technology nodes.

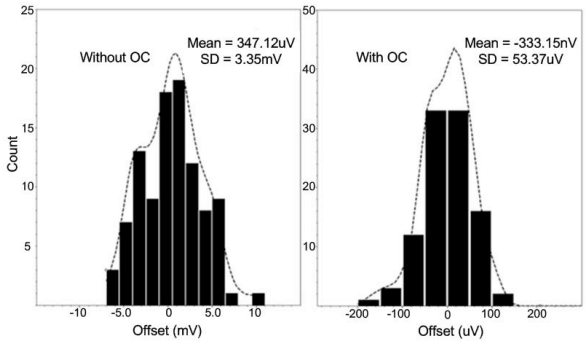

Figure 10. Monte-Carlo simulation results of offset with and without OC

TABLE I. Summary of Performances

Parameter	*Value*
Supply voltage	5 V
Current consumption (at 100KHz clock freq.)	540 nA
Maximum clock frequency	7 MHz
Residual offset	<25 µV
Input referred offset SD (worst case process variation)	53.4 µV
Improvement on offset (worst case process variation)	62.8 X
Area	400x160 µm^2

V. Conclusions

This paper presents a low power dynamic comparator with offset cancellation in a 0.6-µm process. The comparator does not consume any static power and the dynamic current consumption is 540 nA at 100 kHz clock frequency. The novel offset cancellation scheme samples the offset in the time domain and cancels it in a closed-loop fashion with bulk-driven technique. The simulation shows that the residual offset after OC is less than 25 µV, and the input referred offset can be reduced by a factor of 62.8 with worst case process variation.

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