Nano-power tunable bump circuit using wide-input-range pseudo-differential transconductor

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An ultra-low-power tunable bump circuit is presented. It incorporates a novel wide-input-range tunable pseudo-differential transconductor linearised using the drain resistances of saturated transistors. Measurement results show that the transconductor has a 5 V differential input range with <20% of linearity error. The bump circuit demonstrates tunability of the centre, width and height, consuming 18.9 nW power from a 3 V supply, occupying 988 μm^2 in a 0.13 μm CMOS process.

Introduction: Circuits with bell-shaped transfer functions are widely used to provide similarity measures in analogue signal processing systems such as pattern classifiers [1, 2], support vector machines [3] and deep learning engines [4]. Such nonlinear radial basis functions can be realised with the classic bump circuit [5]. However, the original implementation lacks the ability to change the width of its transfer function. Variable width can be obtained by pre-scaling the input voltage before connecting to the bump generator. The pre-scaling circuit using multi-input floating gate transistors [1] or a digital-to-analogue converter [3] consumes area and increase the power overhead. In [2, 6], the widths of bump-like circuits are varied by switching binary-sized transistors, but the number of possible widths is limited. A Gaussian function can be directly synthesised by exponentiating the Euclidean distance [7], but this approach can lead to a complex circuit and large area.

In this Letter, we propose implementing a bump circuit by preceding the current correlator [5] with a tunable transconductor to achieve variable width and height. The design of linear transconductors in subthreshold CMOS is challenging as the linear range of a conventional differential pair diminishes with the gate overdrive, and reaches its minimum in the subthreshold region [8]. Common linearisation techniques such as source degeneration [8], bias offset [9], source coupling [10] and the triode transconductor [11] become either less effective or less practical due to the nano-amp biasing current and exponential transfer function of the transistors. The novel transconductor proposed in this Letter exploits the drain resistance of saturated transistors to obtain a wide-input range and tunable transconductance. The pseudo-differential structure allows operation with a low supply voltage.

Circuit design: The schematic of the proposed bump circuit with a wide-input-range pseudo-differential transconductor is shown in Fig. 1. In the subthreshold, the current correlator $M5$–10 [5] computes a measure of the correlation of its two inputs (with a current scaling factor of 4)

$$I_{\text{out}} = 4\frac{I_1 I_2}{I_1 + I_2} \tag{1}$$

The tunable transconductor ($M1$–$M4$ and I_W) converts the differential inputs V_{in1} and V_{in2} to current outputs $I_1$and I_2. The input transistors $M1$ and $M2$ act as a source follower. In the subthreshold and assuming saturation, their source voltages are given by

$$V_{s1,2} = \kappa V_{\text{in1,2}} - U_{\text{T}} \ln\left(\frac{I_{1,2}}{I_0}\right) \tag{2}$$

where $\kappa \simeq 0.7$ is the gate coupling factor, $U_{\text{T}} \simeq 26$ mV is the thermal voltage and I_0 is the pre-exponential current factor dependent on the process and device dimension. In (2), the first term indicates a linear relationship between $V_{\text{in1,2}}$ and $V_{s1,2}$, whereas the second term causes nonlinearity. This nonlinearity is mild as it is in a logarithm term. $M3$ ($M4$) serves as the current source for follower $M1$ ($M2$); its gate length is intentionally made smaller to exploit its channel length modulation (CLM). With first-order approximation, the drain current in $M3$ is

$$I_{\text{D}} = I_{\text{D0}}(1 + \lambda V_{s1}) \tag{3}$$

where $I_{\text{D}} = I_W + I_1$, λ is its CLM coefficient and I_{D0} is the drain current without CLM, which is equal for both $M3$ and $M4$. We utilise this dependence of I_{D} on V_{s1} to implement a large-value resistor tunable by current I_W. A common mode feedback circuit $M11$–$M14$ controls the gates of $M3$ and $M4$ to provide the common mode rejection for the pseudo-differential structure and ensures that $I_1 + I_2 = I_H$. Combining this with (3), the output currents are

$$\begin{aligned} I_1 &= \frac{2I_W + I_H}{2 + \lambda(V_{s1} + V_{s2})}(1 + \lambda V_{s1}) - I_W \\ I_2 &= \frac{2I_W + I_H}{2 + \lambda(V_{s1} + V_{s2})}(1 + \lambda V_{s2}) - I_W \end{aligned} \tag{4}$$

Assuming a balanced input of $V_{\text{in1}} + V_{\text{in2}} = 2V_{\text{cm}}$, and that the second term in (2) can be neglected, the transconductance is given by

$$\begin{aligned} g_m &= \frac{d(I_1 - I_2)}{d(V_{\text{in1}} - V_{\text{in2}})} = \lambda\kappa\delta(2I_W + I_H), \\ &\text{where } \delta = \frac{1}{2 + 2\lambda\kappa V_{\text{cm}}} \end{aligned} \tag{5}$$

It can be seen that the transconductor is controlled by both I_W and I_H. The V_{cm} term in the δ causes slight asymmetry in the bump transfer function, which is tolerable in typical machine learning applications. The pseudo-differential structure allows a wide differential input range and the circuit can operate at a supply voltage as low as $V_{\text{GS5}} + 6U_{\text{T}}$.

When $V_{\text{in1}} = V_{\text{in2}}$, $I_1 = I_2 = 0.5I_H$ and the maximum bump current output (bump height) is given by $I_{\text{out,max}} = I_H$. With I_H fixed, changing I_W varies the transconductance of the transconductor, and therefore changes the width of the bump. As I_1 and I_2 are linearly related to the input voltages, the shape of the bump output is quadratic

$$I_{\text{out}} = \frac{4}{I_H}\left[\lambda^2\gamma^2(2I_W + I_H)^2(1 + \lambda\kappa V_{\text{in1}})(1 + \lambda\kappa V_{\text{in2}}) - I_W(I_W + I_H)\right] \tag{6}$$

Measurement results: The proposed bump circuit is fabricated in a 0.13 μm CMOS process; thick oxide IO FETs are used to extend the V_{DD}, and therefore the input dynamic range. The active area is 26 × 38 μm^2, as shown in Fig. 2. Biased at $I_W = I_H = 1$ nA and $V_{\text{in1}} = V_{\text{in2}}$, it consumes 6.3 nA current from a 3 V supply. The circuit is functional with V_{DD} down to 0.5 V; however, the input range is limited at such a low supply.

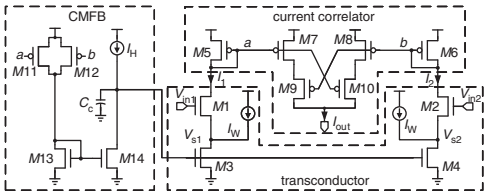

Fig. 1 *Schematic of proposed tunable bump circuit*

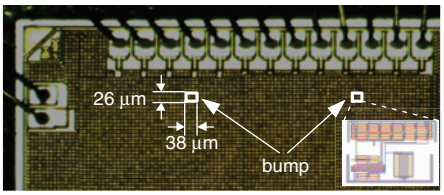

Fig. 2 *Chip micrograph*
Two identical bump circuits are instantiated, covered by metal filles in process; layout view also shown

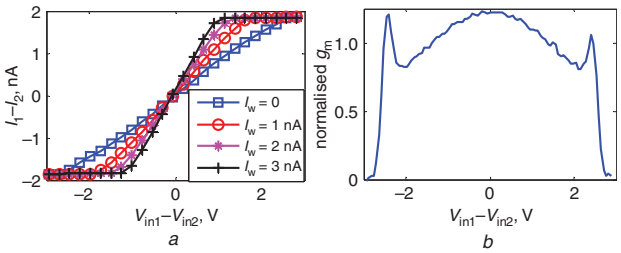

Fig. 3 *Transconductor output and normalised g_m ($I_W = 0$)*
a Transconductor outputs
b Normalised g_m ($I_W = 0$)

The transconductor outputs $I_1$and I_2 are mirrored off chip by two additional PMOSs at nodes a and b, omitted in Fig. 1. The differential output currents with different I_W are plotted in Fig. 3a with $I_H = 2$ nA and balanced input voltage with $V_{cm} = 1.5$ V. The normalised g_m when $I_W = 0$ is plotted in Fig. 3b, showing an input range of 5 V with g_m error below 20%, covering almost the entire input common mode range.

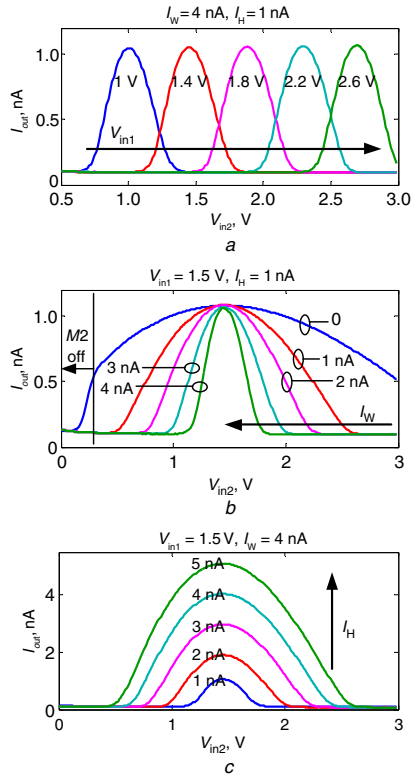

Fig. 4 *Measured bump transfer functions showing variable centre, width, height*

a Variable centre
b Variable width
c Variable height

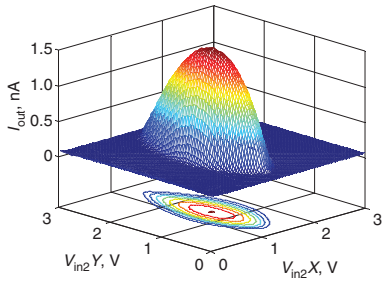

Fig. 5 *Measured 2D bump output with different widths on x and y dimensions*

The nonlinearity can be attributed to the second term in (2), as well as the second-order effects such as the dependence of λ on V_{DS}. It is tolerable in bump generator applications as the bump output itself is an approximation of a highly nonlinear function [1–3, 5, 6]. The offset of about 100 mV is due to the device mismatch and can be calibrated out by utilising floating gate techniques such as that in [12].

The transfer functions of the bump circuit with regard to one input V_{in2} are plotted in Fig. 4, showing variable centre, width and height by varyingV_{in1}, I_W and I_H, respectively. Fig. 4 also demonstrates that the circuit works properly with unbalanced input.

The one-dimensional (1D) bump output can be extended to higher dimensions to represent multivariate probability distribution by cascading multiple bump circuits, i.e. connecting I_{out} of one circuit to the I_H input of the next circuit. The measured 2D bump output is plotted in Fig. 5. Just as in the 1D case, each dimension's parameters are individually tunable.

To evaluate the computational throughput of the circuit, the step response time is measured. With $I_W = I_H = 1$ nA, the output current 95% settling time is 45 µs when the differential input steps from 0 to 1 V.

Table 1summarises the measured performance of the proposed bump circuit. Compared with other recently reported works, the proposed circuit occupies smaller area and consumes significantly lower power.

Table 1: Performance summary and comparison

	This work	[1]	[6]	[7][a]
Technology (µm)	0.13	0.5	0.13	0.18
Supply voltage (V)	3	3.3	1.2	0.7
Power	18.9 nW	90 µW	10.5 µW	485 nW
Area (µm^2)	988	3444	1050	—
Response time (µs)	45	10	—	9.6

[a]Simulation results

Conclusion: We present an ultra-low-power tunable bump circuit to provide similarity measures in analogue signal processing. It incorporates a novel transconductor linearised using drain resistances of saturated transistors. We show in the analysis that the proposed transconductor can achieve tunable g_m with a wide-input range. Measurement results demonstrate a 5 V differential input range of the transconductor with <20% linearity error and bump transfer functions with tunable centre, width and height. We also demonstrate 2D bump outputs by cascading two bump circuits on the same chip.

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One or more of the Figures in this Letter are available in colour online.

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