A Low-Power FSK/OOK Transmitter for 915 MHz ISM Band

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***Abstract*— A PLL-based, low-power, 915 MHz FSK/OOK transmitter is presented. The PLL uses gain-boosted LC VCO and hybrid injection-locked divider topologies to reduce power consumption with acceptable phase noise. In FSK mode, the transmitter consumes 367 µW from a 1.2 V supply with -18.6 dBm output power and achieves maximum 3 Mbps speed (122.3 pJ/bit). In OOK, power consumption is 314 µW with maximum 20 Mbps speed (15.7 pJ/bit). The transmitter occupies 0.29 mm^2 of die area in a 130 nm CMOS process.**

***Index Terms*—915 MHz, transmitter, ISM, low-power, FSK, OOK, gain-boosted, injection-locked.**

I. Introduction

The semiconductor industry has progressed significantly in recent years and allowed consistent improvement of wireless chipsets in terms of functionality, cost, form factor and power consumption. This has enabled a broad range of new short-range, low-power applications, such as wireless sensors. Among all the functions of wireless sensors, communication usually requires most of the power. Therefore, it is important to have an energy-efficient transmitter. In typical wireless sensor networks, transmission range is below 10 m and required radiated power is less than 1 mW [1], for example, maximum 25 µW for MICS band compatible devices. At such low radiated power, the power consumption of the carrier synthesis circuits, rather than the power amplifier (PA), tend to dominate total power consumption.

Direct-modulation transmitter topologies are a popular choice for simple, low-data-rate systems, where the carrier generated by a low-power frequency synthesizer is directly modulated. This reduces the pre-PA circuit complexity and power consumption. Low-power direct-modulation transmitters using unlocked digitally-controlled oscillators have been reported [2], which reduce complexity but require higher power or frequent recalibration to achieve sufficient frequency stability. Injection-locked [3] or RF MEMS resonator-based [4] transmitters are popular for their superior stability at ultra-low power. But this type of structure renders on-chip tuning difficult. Direct-modulation transmitters using phase-locked loops (PLL) for carrier synthesis are also investigated [5] [6]. PLLs offer frequency stability by locking the carrier to a reference frequency and convenient tunability.

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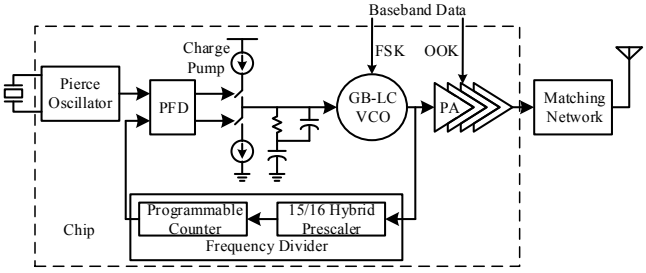

Fig. 1. Architecture of the proposed transmitter.

This paper presents a low-power PLL-based transmitter designed for the 915 MHz ISM band. Section II provides brief descriptions of the different blocks of the proposed transmitter. Measured performance is detailed in section III. Section IV concludes this paper.

II. Transmitter Design

A. 3rd Order PLL

The 3rd-order PLL-based frequency synthesizer is chosen for its simplicity, frequency stability, and easy tunability. The transmitter architecture is shown in Fig. 1. The PLL is designed with about 10 kHz bandwidth, due to low VCO gain in order to reduce PLL spurs. An on-chip Pierce oscillator is used to generate the reference frequency for PLL. It uses only an off-chip, 2.5 mm × 2 mm, 16 MHz crystal and its load capacitance. To achieve 1 MHz channel resolution, the oscillator output is divided down to 1 MHz.

To achieve low-power operation, gain-boosted LC VCO topology, reported in [7], and hybrid frequency divider topology, reported in [8], are used for the two RF blocks.

An FSK modulation system is built into the VCO. Manchester encoding prevents symbol degradation due to the PLL's frequency correction response and also aids in clock and data recovery. An additional OOK modulation system is built into the PA.

B. Gain-Boosted LC VCO

Fig. 2 shows the schematic of the gain-boosted LC oscillator. In this topology, an active gain cell is introduced into a conventional LC oscillator to boost its startup g_m [7]. While conventional LC oscillators consume less power for a given phase noise level than ring oscillators [9], their startup requirements prevent them from taking full advantage of relaxed phase noise requirements of simple low-data-rate radio links. Introduction of the gain cell degrades the frequency stability of the LC oscillator to

some extent, but it still exhibits adequate phase noise performance with low-power operation, comparatively better than ring oscillators. Fig. 3(a) shows a plot of bit error rate (BER) vs carrier phase noise, obtained from system-level simulations (using the MATLAB™ communications toolbox), which indicate that low-data-rate communication systems with simple modulation schemes can tolerate phase noise higher than that in most recently published VCOs.

The GB-LC consists of a G_m cell, a gain cell, and an LC tank. The gain cell is self-biased with a large resistor R_F at its threshold point to provide maximum gain. The G_m cell is dc-coupled to the gain cell. The gain cell and G_m cell have transistor sizes and current density equally ratioed, in order to ensure equal threshold voltages. A single-ended inverter chain operates as a buffer to convert the sinusoid voltage v_{tank} to a rail-to-rail square waveform. A negative feedback loop, comprising M_5, a buffering unity-gain amplifier, and the filter capacitor C_5, prevents non-linear effects, such as unbalanced bias currents from disrupting the G_m cell's bias.

The VCO has three tuning mechanisms - a digital coarse tuning system with about 80 MHz range to counter process variation, a 25 MHz analog tuning system for the PLL and a BFSK (binary frequency-shift keying) system with 250-300 kHz deviation.

Large reduction of power consumption is possible by bringing the bandwidth of the gain cell close to the desired frequency of oscillation. However, the phase delay of the gain-block will cause oscillation to occur at a frequency offset from tank resonance where the tank will be slightly inductive and provide necessary phase lead to counter the delay, as shown in Fig. 3(b). The tank's Q and the bandwidth of the gain cell determine the offset of the oscillation frequency from the resonant frequency. For a suitable tradeoff between power and frequency stability, the oscillation frequency should be in the steep portion of tank phase curve. The frequency of oscillation, f_{osc}, can be estimated from the following equation.

$$f_{osc} = \frac{1}{2\pi}\sqrt{\frac{\omega_c R}{L\left(1+\omega_c R C_{eff}\right)}} \qquad (1)$$

Here R is the equivalent parallel resistance, which depends on the Q of inductor L, C_{eff} the total effective tank capacitance, and ω_c is the gain cell's bandwidth.

C. Hybrid Prescaler

The frequency divider in a PLL can consume considerable amount of power since it runs at full radio frequency. To reduce this power consumption, a low-power divider is used as a prescaler to reduce the operating frequency for subsequent digital blocks. The hybrid frequency divider topology, reported in [8], is used as the prescaler in this work. The schematic of this topology is shown in Fig. 4(a). This topology is based on a single-ended dynamic ring oscillator. Here, propagation of signal

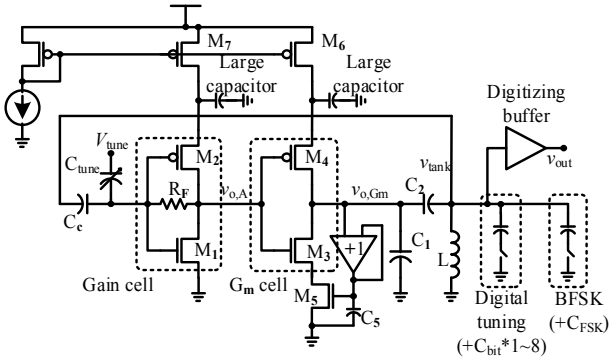

Fig. 2. Schematic of the gain-boosted LC VCO.

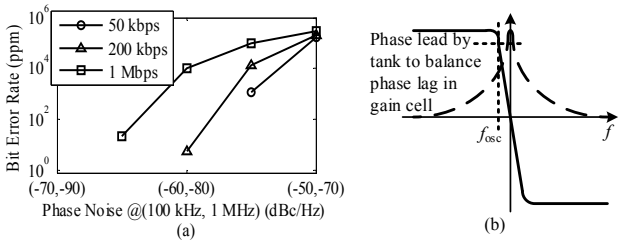

Fig. 3. (a) Simulated bit error rate (BER) of BFSK system with 500 kHz frequency shift for different data rate and carrier phase noise levels. (b) Mode of operation of GB-LC oscillator.

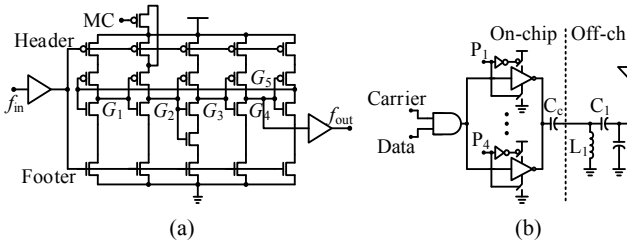

Fig. 4. Schematic of (a) divide-by-4/5 hybrid prescaler and (b) power amplifier with OOK modulation.

through each stage is controlled digitally by the carrier signal from VCO through corresponding header and footer switches in each stage. Thus a prescaler with 5-stage ring core will perform divide-by-5 operation.

The ring-oscillator-based structure of the prescaler allows ultra-low-power operation, such as ILFDs (injection-locked frequency divider). The prescaler also features dual-modulus operation by placing a modulus-control switch which shorts one of the headers to support divide-by-4 mode. The dual-modulus operation allows the division ratio of the feedback loop to be easily programmable and this, along with the coarse tuning in VCO, allows the PLL to be tuned with 1 MHz resolution across the entire 915 MHz ISM band.

Because of its digital mode operation, the prescaler can achieve very wide locking range, similar to conventional digital prescalers, such as TSPC (true single-phase clock) or E-TSPC (extended TSPC). The locking range is determined by the device current leakage at low frequency

and edge times of G_n signals at high frequency. Using minimum-sized devices, locking can be achieved across several sub-GHz frequency range, such as MICS band, 433 MHz and 915 MHz ISM bands, with very low power consumption.

D. Power Amplifier

At low output power levels, typical of short-haul wireless sensors, simple PA design and operation is desirable to reduce power consumption of driver circuits and use small matching networks. In this work, an inverter-based power amplifier is implemented, which is shown in Fig. 4(b). The digitized carrier signal drives four identical inverter stages in parallel, which drive an off-chip matching network. A coupling capacitor, C_c, prevents the network from disrupting the DC bias of the inverter. The output power can be varied by turning the stages on or off. The maximum output power achieved is -18.6 dBm, and can be reduced to -29.6 dBm. With high-Q off-chip components, the -3 dB bandwidth of the network is about 45 MHz.

To enable on-off keying (OOK) modulation, the carrier is ANDed to the baseband data before it drives the PA.

III. Measurement Results

The proposed low-power transmitter is fabricated in a 0.13 µm 1P8M CMOS process. Fig. 5 shows the microphotograph of the transmitter. The PLL with its bias network, crystal oscillator (XO) and power amplifier occupies 0.29 mm^2 silicon area. This area excludes the pad-driving RF test buffer and other circuits used only for testing purposes. The foundry-modeled, on-chip, 15-turn, 37 nH inductor in the VCO occupies 220 × 220 µm^2 area.

Fig. 6(a) shows the output spectrum of the unmodulated 925 MHz carrier generated by the proposed transmitter. The maximum output power is -18.6 dBm with 12.5% drain efficiency, achieved by turning on all four PA stages. The output power can be reduced to minimum -29.67 dBm with 3% drain efficiency, using one PA stage.

The phase noise spectra of the free-running GB-LC VCO and the PLL is shown in Fig. 6(b). The PLL suppresses close-in phase noise in about 10 kHz closed-loop bandwidth. Phase noise is -100.2 dBc/Hz at 1 MHz offset.

Fig. 7 and Fig. 8 show the performance of the BFSK and OOK modulation systems respectively. The BFSK modulation with 250 kHz deviation achieves maximum

TABLE I
POWER BREAKDOWN OF PROPOSED TRANSMITTER

Block	Power (µW)
Crystal oscillator	32.6
PLL (=PFD + Charge-Pump + Freq. Divider)	50.1
GB-LC VCO + Bias network	174
Power Amplifier (FSK/ OOK)	110.4/ 57.6
Total (FSK/ OOK)	367.1/ 314.3

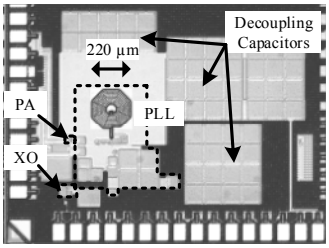

Fig. 5. Microphotograph of a bare die containing the fabricated transmitter. Total area occupied by the transmitter is 0.29 mm^2. This excludes circuits used only for testing purposes, such as RF pad-driving buffer.

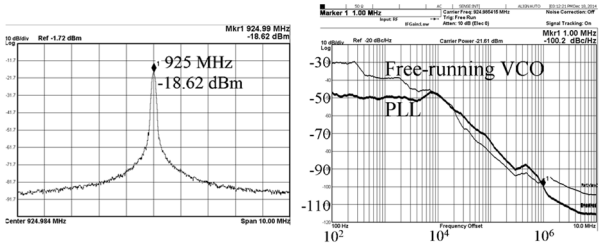

Fig. 6. (a) Spectrum of unmodulated 925 MHz carrier signal, with PA at maximum output power, -18.6 dBm. (b) Phase noise spectra of the PLL and the free-running VCO. Phase noise of PLL is -100.2 dBc/Hz at 1 MHz offset.

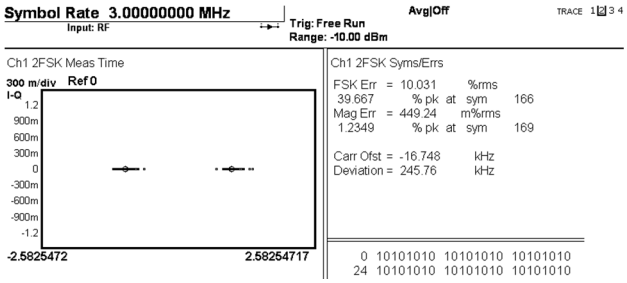

Fig. 7. Constellation diagram and BFSK error results of the proposed transmitter. The 925 MHz carrier is BFSK-modulated with a 1.5 MHz square wave, simulating a 3 Mbps '01010101' bitstream. RMS FSK error is about 11%. OOK is disabled.

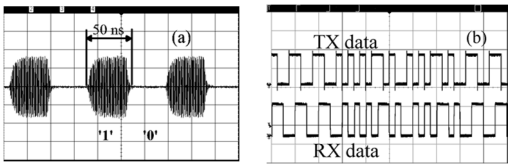

Fig. 8. (a) 925 MHz carrier OOK-modulated by 10 MHz square wave (20 Mbps bitstream). (b) Manchester-encoded random data transmitted at 50 kbps and received at 1 m distance through OOK modulation.

3 Mbps data rate with 11% rms error, adequate for most low-cost wireless applications [10]. BER can be predicted from this data by calculating the probability of a random variable, in a Gaussian distribution with 0 mean and 11.5% standard deviation, to be greater than 0.5. Thus BER is calculated to be 2.74 ppm. The measurement is performed with a 1.5 MHz square wave, simulating a '01010101'

TABLE II
PERFORMANCE SUMMARY AND COMPARISON TO RECENT WORKS

	This work		[2]	[3]	[5]	[6]	[11]
Frequency (MHz)	925		920	400	400/433	2400	400
CMOS Tech. (nm)	130		180	130	130	90	90
Die area (mm^2)	0.29		-	0.04	0.41	0.882	0.06
Architecture	PLL + PA		Unlocked DCO + PA	ILVCO + Edge-combining PA	PLL + PA	PLL+PA	ILVCO + Edge combiner + PA
On-chip channel selection	Yes		Yes	No	Yes	Yes	No
Output power (dBm)	-18.6		-10	-16	-16	0	-17
Modulation	FSK	OOK	FSK	FSK	FSK	OOK	OOK
Data rate (Mbps)	3*	20	5	0.2	0.08	10	1
Power consumption (μW)	367	314	700	90	150	2530	160
Energy efficiency (pJ/bit)	122.3	15.7	140	450	1875	253	160
Supply voltage (V)	1.2		0.7	1.2	0.7-1.2	1	0.6

* 11% rms FSK error, reduces to 4.4% at 200 kbps data rate.

bitstream at 3 Mbps. At 200 kbps data rate, the rms error reduces to 4.4%. The OOK system is tested with up to 20 Mbps data rate. A pseudo-random data set of about 4.7 million bits is also transmitted at a receiver-limited rate of 50 kbps and received at 1 m distance with 0 bit errors. Manchester encoding is used for clock recovery and removing DC state from data.

The proposed transmitter consumes 367 μW power from a 1.2 V supply in BFSK mode with -18.6 dBm output. In OOK mode with continuous '01010101' data, the power consumption is 314 μW. A breakdown of the total power consumption is shown in Table I.

IV. CONCLUSION

A low-power, PLL-based, FSK/OOK transmitter is proposed for 915 MHz ISM band applications. PLL-based architecture allows better stability than unlocked DCO-based transmitters and easy tunability compared to injection-locked structure. Power reduction of the PLL is achieved using gain-boosted LC VCO and hybrid prescaler topologies. Compared to recent works, as shown in Table II, this transmitter achieves superior energy efficiency in both modulation schemes with high data rate. In FSK mode, the transmitter can achieve maximum 3 Mbps data rate with only 11% rms error (equivalent to 2.74 ppm BER) and 367 μW power consumption. In OOK mode, the transmitter is tested at up to 20 Mbps data rate with only 314 μW power consumption. Thus, this transmitter is very suitable for low-power wireless sensor applications.

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