NeuralWISP: An Energy-Harvesting Wireless Neural Interface with 1-m Range

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***Abstract*— We present the NeuralWISP, a wireless neural interface operating from harvested RF energy. The NeuralWISP is compatible with commercial RFID readers and operates at a range up to 1m. It includes a custom low-noise, low power amplifier IC for processing the neural signal and an analog spike detection circuit for reducing digital computational requirements and communications bandwidth. Our system monitors the neural signal and periodically transmits the spike density in a user-programmable time window. The entire system draws an average 20μA from the harvested 1.8V supply.**

I. Introduction

Neural interfaces have made tremendous technology-driven advances in the recent past. Cochlear implants are an early example of clinically relevant implantable devices [1], modern electronics are enabling previously impossible brain research experiments [2], and major progress has been made toward neurally controlled prosthetics [3]. Because transcutaneous wiring poses a significant infection risk, it is desirable that a neural interface communicate and receive power wirelessly. Previous systems [4][5] have achieved wireless operation by using a near-field inductive link to transmit power and data. However, these systems require that the external coil be located within a few centimeters of the internal coil. A wireless neural interface with a range of 1m or more will enable the removal of the interrogator from the head and would allow wireless interfaces to be placed on small animals incapable of carrying the interrogator hardware, such as mice.

We present a wireless neural interface which harvests power from the radio-frequency (RF) energy provided by a standard commercial UHF RFID reader. The system operates at a distance of up to 1m from the reader. It records the spike count in a programmable window (typically 1-10s) and subsequently transmits the spike count to the reader as part of the tag identification number that the reader is designed to acquire. This allows the neuroscientist a wireless, battery-free method of recording spike density ($\frac{spikes}{second}$) as various tasks are performed or stimuli are presented.

II. System Design

The NeuralWISP builds upon our prior work on the Wireless Identification and Sensing Platform (WISP) [6][7]. The WISP is a fully-passive UHF RFID tag that uses an ultra-low power, 16-bit, general-purpose microcontroller (μC) for sensing, computation and RFID communication. The use of a programmable μC allows WISP to be easily configured for different applications including measurement of temperature, light level, strain, and acceleration [6]. In monitoring applications, analog sensor outputs change slowly and thus permit periodic, low-frequency (1 to 50 Hz) measurement. However, a much faster sampling rate (at least 8 kHz) is necessary to detect neural spikes. Achieving this sampling rate under the constraints of the limited power budget of an RFID tag is not possible with general purpose microcontrollers available today.

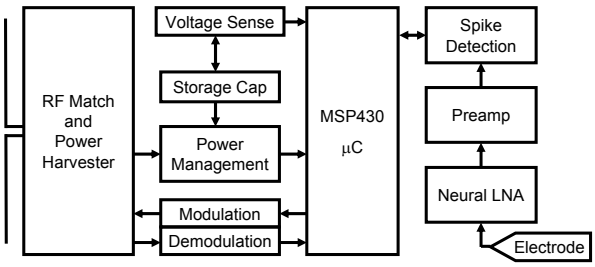

Fig. 1. Block diagram of NeuralWISP.

In order to minimize the average current consumption, a continuous-time analog spike detector was designed to generate a μC interrupt when a spike occurs. This allows the μC to remain in a low-power sleep mode during periods of inactivity and only wake up to process spikes or communicate with the RFID reader. The μC counts spikes during a programmable window and is reset after the spike count is transmitted to the reader.

The architecture of the NeuralWISP is shown in Fig. 1. Like a typical RFID tag, power is received at the antenna, voltage-multiplied, rectified, and regulated to provide a stable system power supply. The design and performance of the energy harvesting circuitry is described in detail in [6][7]. The neural input signal is amplified and applied to an analog spike detector in addition to an analog-digital converter (ADC) integrated in the μC. The μC performs the control and timing tasks, and implements the RFID communication protocol.

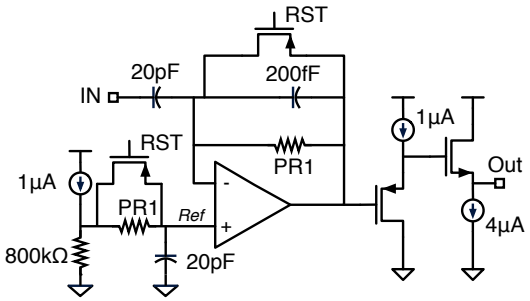

Fig. 2. Schematic of custom 8 μA low noise neural amplifier fabricated in a $0.5\mu m$ SOI CMOS process

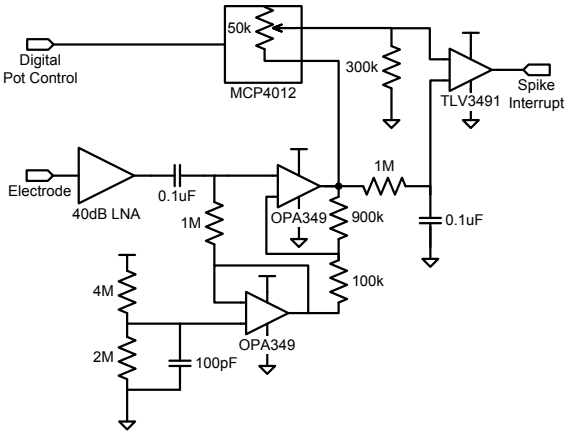

Fig. 3. Analog front end circuitry, including custom LNA, 20dB pre-amp, and spike detector with programmable threshold

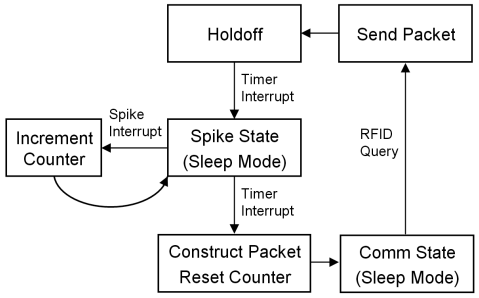

Fig. 4. Software state diagram. The μC is in the low-power Spike State for the majority of the time, awakening only to increment the spike counter after a detection or to communicate with the reader.

A. Analog Signal Path

The extremely low signal levels recorded from neural probes place severe constraints on the analog front-end. Input-referred noise levels must be $< 10\mu V_{RMS}$ while providing good linearity and high gain. These requirements typically result in the low noise neural amplifier consuming a majority of the system power. In the NeuralWISP, the power dissipation limits the wireless range, so power must be minimized. We designed a custom low-noise amplifier (LNA) in a 0.5µm SOI BiCMOS process to meet these requirements. The amplifier is designed to provide a gain of 40dB. A schematic is shown in Fig. 2. The amplifier is built using a two-stage op-amp with capacitive feedback. A closed-loop configuration was chosen for this system because open-loop amplifiers, while demonstrating superior noise efficiency factors (NEF), typically suffer from inferior power-supply rejection [8]. MOS-bipolar pseudo-resistors [9] (PR) were used to set a sub-Hz low frequency pole for DC rejection. For small signals, the PRs have an incremental resistance of about $10^{12}\Omega$, resulting in a time constant of several seconds. In order to avoid long settling times on power up, a power-on-reset circuit is included on chip which temporarily shorts out the pseudo-resistors. The high-pass corner frequency set by the pseudo-resistors is much lower than is necessary for the extra-cellular recording task being demonstrated here. However, transconductor implementations of high-valued resistors consume additional power and contribute noise. A source-follower output stage was chosen for its flexibility with respect to load conditions. A resistive load to ground will increase the current in the NMOS source follower transistor, allowing the amplifier to automatically adapt to resistive loads without consuming extra static bias current under lightly loaded conditions or using a complicated class AB output stage. The chip is completely self-contained, and includes a supply-independent bias current generator allowing consistent operation over a range of 1-5V.

An additional gain of 20dB is provided by a second amplifier built from two OPA349 op-amps, shown in Fig. 3. The first opamp is used to establish a 0.6 V reference for AC coupling the amplifier stages, and the second opamp is used in a non-inverting gain configuration. The gain of the first stage allows relatively noisy micro-power op-amps to be used for the second gain stage. Consequently, the second stage consumes only 1.9 μA from a 1.8 V supply, including the reference.

The output of the second amplifier is connected to the ADC input of the MSP430 microcontroller to allow for direct digitization of the neural signal. Additionally, the amplified signal is applied to an analog spike detector. The signal is low-pass filtered with a time constant of 0.1 s to generate the detection threshold. The signal is also attenuated and shifted towards 0 V by up to 15% via a variable-ratio resistive divider. A digitally-controlled resistor, variable from 0Ω-50kΩ, determines the attenuation of the divider and thus the sensitivity of the spike detector. The spike detector's programmable threshold allows adjustment for dynamic neural signals and noise levels.

B. Digital Control

An MSP430F2274 microcontroller (μC) is used to implement control, timing, and communication tasks. Fig. 4 shows the software architecture. On bootup, the μC configures the adjustable resistor in the spike detector. During the primary mode of operation, the μC will count spikes during a user-specified time interval (typically 1-10s) and transmit the number of spikes detected at the end of the interval. During the counting interval, the μC is in a low-power sleep state for the majority of the time. The spike detector triggers an interrupt, which causes the μC to wake up, increment the spike count, and return to sleep. A timer drives another interrupt, which

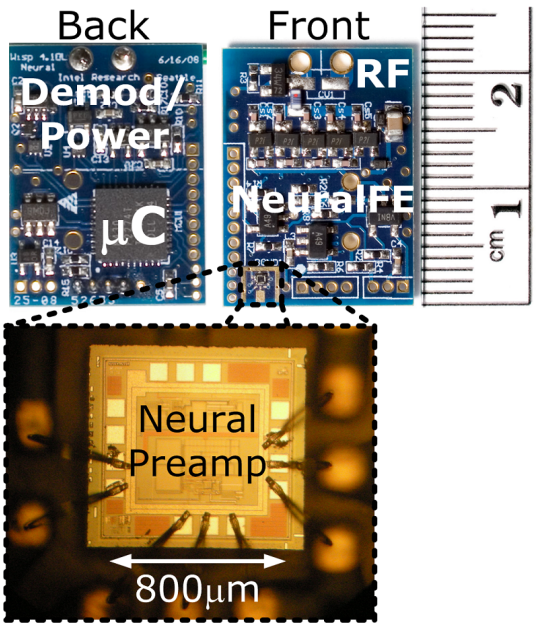

Fig. 5. System photograph. Inset shows chip-on-board mounting of the custom low-noise amplifier IC.

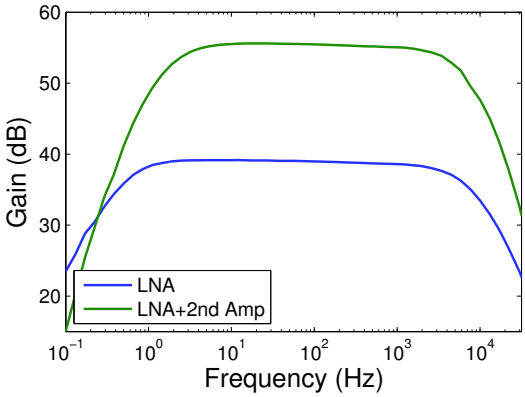

Fig. 6. Gain versus frequency for both low-noise amplifier (LNA, bottom), and the combined gain of the LNA and 2nd amplifier.

signals the end of the counting interval, causing the μC to exit the spike-counting mode and await a communication session with the reader. After communicating with the reader, the μC pauses for 3s to allow the analog circuits to recover from RF interference that occurred during the read, then returns to the spike counting phase and repeats the cycle.

III. Experimental Results

The fabricated board is shown in Fig. 5. The populated board alone weighs 1.0g, and a 900 MHz wire dipole antenna (not shown) weighs approximately 0.6g. During spike counting, the system draws an average of about 20µA of current from its unregulated supply, of which 8µA is consumed by the neural pre-amp. A commercial RFID reader with +30dBm transmitted power was used to wirelessly supply power and communicate with the NeuralWISP.

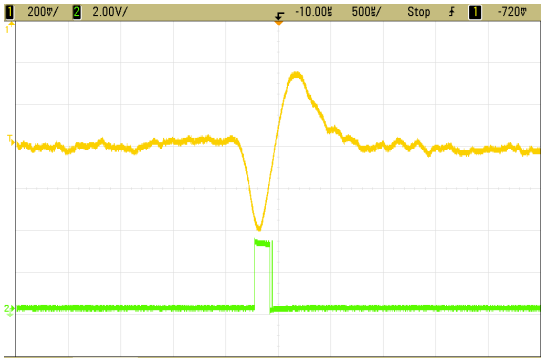

Fig. 7. Operation of the spike detector. The input signal (top) has been amplified by 1000x for oscilloscope viewing. The amplitude at the input to the NeuralWISP is approximately 800µVpp.

Input-referred noise of the low-noise amplifier is $4.4\mu V_{RMS}$, measured from .25Hz to 25kHz. Operating from a supply between 1V and 5V, the LNA provides a measured gain of 39dB with a bandwidth spanning 0.5Hz to 5.9kHz. Current consumption at 1.8V is 8µA, including the bias generator and output buffer. Fig. 6 shows the frequency response of the first stage and the combined response of both gain stages. The LNA combined with the second amplifier provides a mid-band gain of 56dB with a bandwidth from 2Hz to 4.9kHz.

To characterize the spike detector, we applied a synthesized neural recording [10] to the NeuralWISP input. This technique allowed us to vary the SNR and spike rate in the recording and provided a reference against which to compare our measured spike detection results in order to characterize the detector accuracy. Fig. 7 shows the operation of the detector on a single spike, with an 800 μV_{P-P} input signal. The interrupt duration can be configured to ensure that any glitches in the spike detection signal do not cause errors in the spike count.

Fig. 8 shows the spike detector accuracy. Spikes were detected using the hardware analog spike detector (circle tick) and also using a PC-based threshold-crossing detector (square tick) for comparison. Both detectors were run on synthetic recordings with an amplitude of approximately $400\mu V_{P-P}$ and SNR of 10dB (left) and 6dB (right). The results were compared with the known spike times provided by the signal synthesis software. The analog detector demonstrates comparable discriminative abilities to the software detector, indicating that noise contributions from the analog front end do not limit spike detection performance.

Fig. 9 demonstrates the operation of the NeuralWISP. The middle trace is the unregulated voltage stored on a 100µF capacitor, which begins at 0V, since the WISP starts out with no stored energy. Initially, the reader is configured to transmit power in continuous-wave (CW) mode, which charges the storage capacitor to 5.5V where it is clamped by a zener diode. As the stored voltage rises, the μC boots up (A). At point (B) continuous-wave transmission stops and the RFID reader reads data from the WISP. The first read following bootup will contain empty data. Following the read, the μC enters a

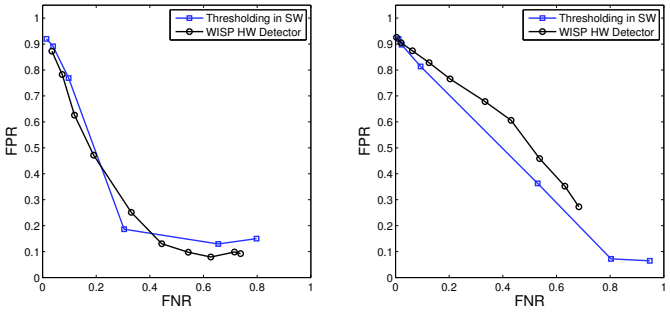

Fig. 8. Accuracy of the spike detector compared to a software spike detector for SNR=10dB (left) and SNR=6dB (right). The x-axis is the false negative rate (FNR = Number of missed spikes / Number of total true spikes). The y-axis is the false positive rate (FPR = Number of false detections / Number of total detections).

Fig. 9. Two read cycles of wireless operation, showing the spike detector output (top), the unregulated stored voltage (middle), and a microcontroller output (bottom) pulsed to show operation. The data was taken at a distance of approximately 1m from the reader.

3s waiting state (C) in order to allow the analog circuits to recover from RF interference which occurred during the read. After 3s, the WISP begins counting spikes (D) for 5s. After the spike-counting phase, the reader again transmits CW power (E) to recharge the storage capacitor, followed by another read, which retrieves data from the previous spike-counting phase (D). This cycle is repeated indefinitely.

The NeuralWISP could also be configured to sample spike waveforms after a spike is detected, and transmit the digitized data. An appropriate duty cycle would need to be chosen in order to meet the constraints imposed by the data rate allowed by the tag/reader interface. Fig. 10 shows a spike captured and digitized by the NeuralWISP. The data received at the reader is superimposed on the original spike waveform. This experiment demonstrates that accurate reconstruction of the spike can be accomplished by waking the μC and ADC from low-power sleep after spike detection, dramatically reducing average system power.

IV. Conclusions

We have demonstrated the NeuralWISP, a wirelessly powered neural interface with a range of 1m. Using harvested RF power, our system transmits spike counts to a commercial RFID reader at user-programmable intervals.

By operating from a wireless power source, the NeuralWISP allows indefinite operation without the need to change batteries, a critical need for implanted neural interfaces. The platform is also flexible and can be programmed to operate in different modes, such as spike time-stamp recording, or continuous recording on a duty-cycled basis.

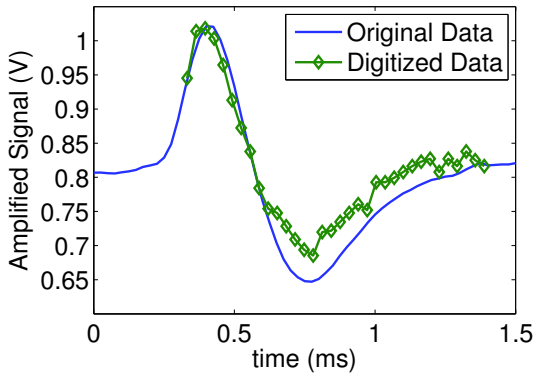

Fig. 10. A single spike digitized by the on-board ADC. The μC began sampling and converting in response to an interrupt from the spike detector.

V. Acknowledgements

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