A 167 µW 915 MHz Gain-Boosted LC VCO

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***Abstract*— This paper presents the design and performance of a gain-boosted LC voltage-controlled oscillator (VCO) topology for ultra-low-power applications. This novel topology is a combination of conventional LC and ring oscillators which facilitates much lower startup power requirement than conventional LC oscillators, allowing ultra-low-power operation with acceptable phase noise performance for low-data-rate applications. Measurements show about 167 µW power consumption from 1.2 V supply when operating at 915 MHz and the phase noise is measured to be -97.9 dBc/Hz at 1 MHz offset. The VCO has a 4-bit digital tuning range of about 80 MHz and an analog tuning range of at least 22.5 MHz. The VCO also has a FSK modulating system with 550 kHz/bit shift. The VCO is realized in 0.13 µm CMOS process and occupies 0.26 mm^2 of area.**

***Index Terms*—915 MHz, LC VCO, ISM, low-power, FSK VCO, gain-boosted, phase noise.**

I. Introduction

THE need for highly integrable and low-power frequency synthesizers for implantable and body-worn wireless medical devices is continuously growing. As a result, low-power design of phase-locked loop frequency synthesizer with acceptable noise performance is becoming more desirable by the day. Typically, the voltage-controlled oscillator (VCO) and frequency divider dominate power consumption, since they run at full carrier frequency.

Performance improvement of the two common topologies of VCOs is well documented in the literature. The LC VCOs are still very popular for their superior phase noise performance and lower supply-sensitivity than ring oscillators. But due to low quality factors of on-chip inductors, active parts of the LC VCOs need high power to counter the loss in the LC tanks. This puts a hard limit on reduction of minimum startup power of the LC VCOs. The LC VCO, used in [1], consumes 300 µW power from a 0.7 V supply, operating at 400 MHz MICS band with -118 dBc/Hz phase noise at 1 MHz offset. In [2], phase noise is improved by switching tail current at reduced duty cycle to reduce flicker noise, where the VCO operates at 5.36 GHz with 3 mW power and -121.3 dBc/Hz phase noise at 1 MHz offset. LC VCOs also suffer from limited tuning range.

On the other hand, ring-type oscillators offer easy integration, since they don't require any space-consuming inductor. They also have high tunability which is useful to counter process and temperature variations. But at the same time, they are known to have inferior frequency stability than LC oscillators and therefore require considerable power to achieve acceptable phase noise [3]. For example, the ring VCO in [4] has a very large tuning range (0.2 – 2.1 GHz) with -90 dBc/Hz at 100 kHz offset, but consumes 7.01 mW power operating at 1.2 GHz. Another 900 MHz ring oscillator, in [5], shows phase noise of -105.5 dBc/Hz at 600 kHz offset with 15.4 mW power consumption. Recently, a 90 µW MICS band transmitter is reported [6], which uses a 45 MHz ring oscillator to be frequency-multiplied at output by an edge-combiner power amplifier. The ring oscillator achieves excellent phase noise performance (less than -120 dBc/Hz at 1 MHz offset), when injection-locked to an external 45 MHz crystal. This structure does not allow on-chip frequency tuning, thus no channel-selectivity, and can only operate at a fixed frequency in the MICS band or 433 MHz ISM band, depending on the external crystal used.

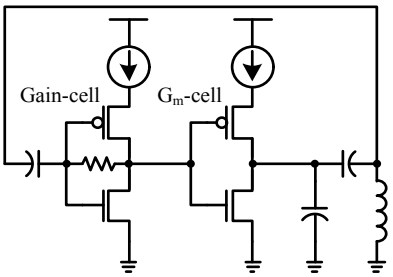

Fig. 1. Simplified schematic of the proposed hybrid VCO.

However, it can be shown that simple modulation systems require only modest frequency stability and low-data-rate digital modulation systems are able to tolerate higher phase noise than that in most of the recently published VCOs. Fig. 2 shows a plot of bit error rate (BER) for different oscillator phase noise levels and data-rates for a 2-FSK modulated system with 500 kHz frequency shift. This plot is obtained from a simulation using the MATLAB communication toolbox. It shows that a 200 kbps 2-FSK system yields a BER of only 5.5 ppm with carrier phase noise as high as -60 dBc/Hz and -80 dBc/Hz at respectively 1 kHz and 1 MHz offsets. BER increases with data rate. This shows that for simple low-data-rate communication systems, phase noise of the carrier or VCO can be compromised as a trade-off for low power consumption.

In this paper, we describe a novel topology for oscillator design. Fig. 1 shows a simplified schematic of the proposed gain-boosted LC (GB-LC) VCO. This VCO is a combination of a conventional common-source LC oscillator and a gain cell

Manuscript received October 1, 2012. This work was supported by the National Science Foundation (DBI-1152361).

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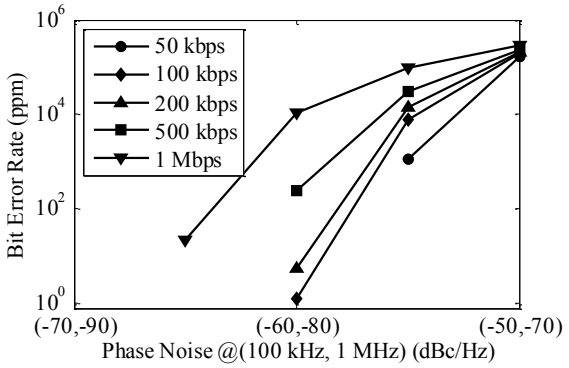

Fig. 2. Bit error rate (BER) of 2-FSK system with 500 kHz frequency shift for different data rate and carrier phase noise levels.

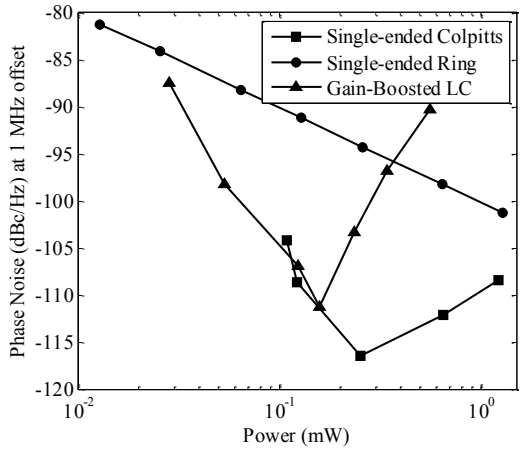

Fig. 3. Simulated phase noise of 1 GHz signals, at 1 MHz offset, generated by a single-ended ring oscillator, a single-ended Colpitts oscillator and the proposed GB-LC oscillator for different core power consumptions from 1.2 V supply.

from single-ended ring oscillators. This hybrid structure offers frequency stability superior to a ring oscillator, while the delay cell introduced in the loop provides extra active gain at much lower power consumption than LC oscillators. Fig. 3 shows comparison between simulated phase noises of 1 GHz signals, at 1 MHz offset, generated by a single-ended Colpitts oscillator, a single-ended ring oscillator and the proposed GB-LC oscillator for different power consumptions from 1.2 V supply. The proposed oscillator, with its moderate phase noise and low startup criteria, fills the gap between the high-noise, low-power ring oscillator and low-noise LC oscillator whose power consumption reduction is limited by startup criteria. This oscillator is designed and fabricated in a 0.13 µm, 1P8M CMOS process. Measurements show about only 167 µW of power consumption from a 1.2 V supply while operating at 915 MHz with -97.9 dBc/Hz phase noise at 1 MHz offset. Section II describes the structure of the proposed GB-LC VCO. Analysis for estimating frequency of oscillation and oscillation criteria and discussion on phase noise performance are described in section III. The measured performance of the fabricated oscillator is shown in Section IV. Section V gives the conclusion.

II. VCO Structure

A. Core Structure

The core structure of the proposed GB-LC VCO and how it's derived from conventional negative-g_m oscillator are shown in

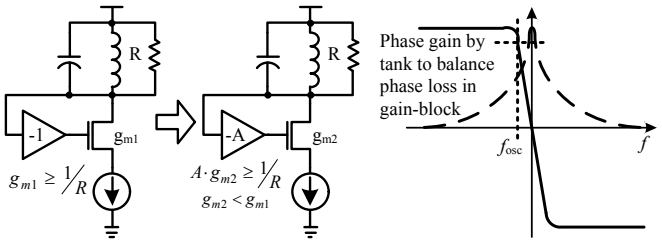

Fig. 4. Derivation of core structure of the proposed VCO and frequency of oscillation.

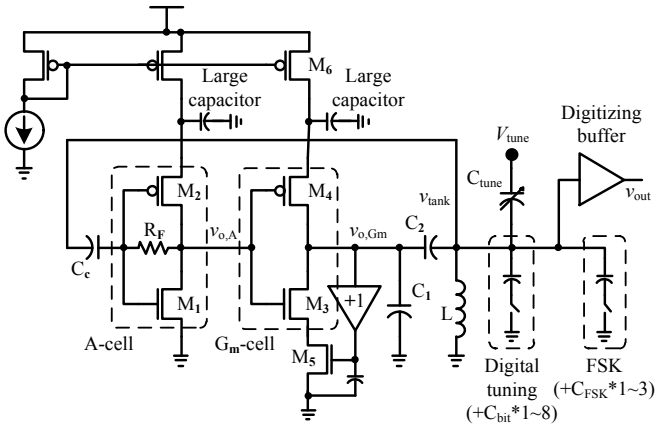

Fig. 5. Detailed schematic of the proposed gain-boosted LC VCO.

Fig. 4. Introducing a gain block in the loop reduces g_m required to counter the energy loss in an on-chip low-Q LC tank, thus reducing minimum startup power requirement. Also, the gain block, driving only the gate capacitance of the g_m-device, can achieve a given gain with much lower power consumption than the transconductor in a conventional LC oscillator. Thus reduction of total power consumption can be achieved. Large reduction of power consumption is possible by bringing the bandwidth of the gain-block close to the desired frequency of oscillation. However, the phase delay of the gain-block will cause oscillation to occur at a frequency offset from tank resonance where the tank will be slightly inductive and provide necessary phase lead to counter the delay. This offset will be determined by tank's Q and the bandwidth of the gain-block. Optimum power reduction will be achieved when the oscillation frequency will settle in the steep portion of tank phase curve where frequency sensitivity to noise is the least.

A detailed schematic of the proposed oscillator is provided in Fig. 5. The core structure consists of a "G_m-cell" and a gain block "A-cell". A-cell is self-biased with a large resistor R_F at its threshold point where it provides maximum gain. The G_m-cell is dc-coupled with A-cell and is proportioned with A-cell in device-size and bias currents to have the same threshold point. The tail current sources have large capacitances at outputs to form low-pass filters for supply noise with very low corner frequency. C_c and C_2 decouples the two cells from inductor so it doesn't disrupt their bias conditions. The corner frequency from C_c and R_F should be much less than the oscillation frequency. A digital single-ended inverter chain operates as buffer to convert the sinusoid voltage v_t to square waveform. The input capacitance of the buffer is small compared to tank capacitance and does not affect the core loop.

B. G_m-cell Bias Stabilization

After oscillation starts, the current of the G_m-cell increases to compensate for energy loss in the LC tank. As a result, the V_{DS} of M_6 increases and this pushes $V_{o,Gm}$ lower, destroying the bias condition of G_m-cell. As a result, oscillation cannot sustain. To address this problem, M_5 is added to this cell. M_5 is controlled by the dc average of $v_{o,Gm}$ and keeps it near the threshold point of G_m-cell.

C. Tuning

The proposed VCO includes two tuning systems and an FSK modulation system. All three systems change the tank capacitance to change the tank resonance frequency and thus oscillation frequency is tuned.

The digital tuning system consists of 8 equal-sized capacitances controlled by a 4-bit word and provides a 9-step tuning. With tuning code '0', all the capacitors are switched off and oscillator frequency is highest. With codes '1' – '8', the corresponding number of capacitors is switched on and adds to the equivalent tank capacitance and lower oscillation frequency. This system provides about an 80 MHz tuning range with the 902 – 928 MHz ISM band at center, which is sufficient to counter process variations.

The analog tuning system consists of a varactor, C_{tune} connected to the tank. It is controlled by a rail-to-rail (0 – 1.2 V) input voltage, V_{tune} and frequency is highest when $V_{tune} = 0$ V and vice versa. The frequency range of analog tuning, and hence sensitivity is affected by the digital tuning configuration and C_{tune} is sized so the tuning range varies within 22.5 – 30.2 MHz, which almost covers the 915 MHz ISM band. This tuning system is non-linear.

The FSK modulation system is similar to the digital tuning system. It consists of three small, equal, switched capacitors. When FSK input is logic high, one of these capacitors is connected in parallel to the tank and reduces oscillation frequency by about 550 kHz. This shift can be increased by turning on two (1.2 MHz) or all three (1.825 MHz) capacitors.

III. Analysis of the Design

A. Estimation of Oscillation Frequency

The GB-LC VCO would operate similar to a conventional negative-g_m oscillator at the LC tank resonance frequency provided that the A-cell has bandwidth much higher than the resonance frequency. In this case, the two cells will each provide 180º phase shift and total phase shift would be 360º around the loop. But to reduce the power consumption, the bandwidth is brought down close to the oscillation frequency. As a result, phase shift from A-cell would be more than 180º and oscillation frequency will be slightly lower than resonance frequency where the tank will provide phase lead to cancel the extra phase delay. The frequency of oscillation can be thus determined by estimating the phase lead and lag from the tank and A-cell respectively. AC equivalent circuits of these two parts, necessary for this estimation, are shown in Fig. 6. For simpler calculation, the 180º phase shifts of the two cells will be ignored as they cancel out each other and only the excess phase will be calculated.

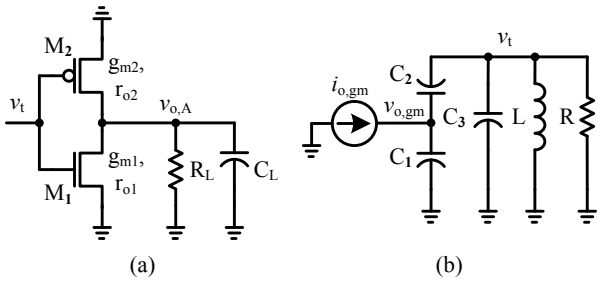

Fig. 6. AC equivalent circuits of the A-cell (a) and LC tank (b) for estimating oscillating frequency with phase-balance equation.

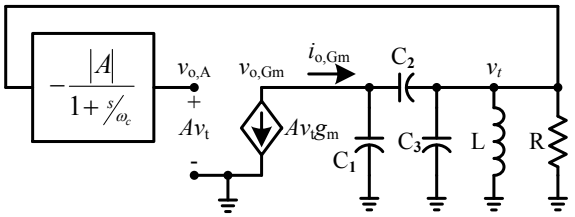

Fig. 7. Small-signal equivalent circuit of the proposed GB-LC oscillator core.

The phase delay of the A-cell can be determined from its transfer function, which is given by the following equations.

$$A = \frac{|A|}{1 + j\omega/\omega_c} = \frac{|A|}{1 + j\omega R_L C_L} \tag{1}$$

$$|A| = (g_{m1} + g_{m2})(r_{o1} \| r_{o2}) \tag{2}$$

$$R_L = r_{o1} \| r_{o2} \| \left(\frac{R_F}{1 + 1/|A|} \right) \tag{3}$$

$$C_L = C_{i,Gm} + C_{RF}/2 + C_{dg,A}(1 + 1/|A|) \tag{4}$$

Here $C_{i,gm}$ is the input capacitance of G_m-cell, C_{RF} is parasitic capacitance of poly-resistor R_F and $C_{dg,A}$ is the drain-gate capacitance of A-cell. With the values of design parameters of the proposed oscillator, $|A|$ and ω_c are calculated to 12.493 V/V and 7.5457 Grad/s. The phase delay of A-cell is given by

$$\theta_A = -\tan^{-1}\left(\omega/\omega_c \right) \tag{5}$$

The output current of the G_m-cell, $i_{o,gm}$ is in phase with $v_{o,A}$, if the 180º phase shift is ignored. The phase lead in v_t from $i_{o,gm}$ or $v_{o,A}$ would be the phase angle of the LC network, θ_t. Here, C_1 and C_2 are metal-to-metal capacitors and C_3 and R is given by the following equations.

$$C_3 = C_{2,bot} + C_{c,bot} + C_P + C_{i,A} + C_{RF}/2 \tag{6}$$

$$R = R_P \| \left(R_F / 1 + |A| \right) \tag{7}$$

Here, $C_{2,bot}$ and $C_{c,bot}$ are bottom-plate capacitances off C_2 and C_c, C_P is the parasitic capacitance of inductor L, $C_{i,A}$ is the input capacitance of A-cell. R_P is the equivalent parallel tank resistance. Mid-band gain $|A|$ is used in (3), (4) and (7) to simplify the analysis. v_t is given by the following equation.

$$v_t = i_{o,gm} \cdot \frac{R \| sL \| 1/sC_3}{1 + C_2/C_1 + sC_1(R \| sL \| 1/sC_3)} \tag{8}$$

θ_t can be determined from (8) as in the following expression.

$$\theta_t = \tan^{-1}\frac{R\left(1-\omega^2 LC_{eff}\right)}{\omega L} \tag{9}$$

Here, $C_{eff} = C_3 + \frac{C_1C_2}{C_1+C_2}$. Oscillation will occur at a frequency where θ_t and θ_A balances each other so the total phase shift around the loop is zero.

$$\theta_t + \theta_A = 0 \tag{10}$$

Equation (11) may be referred to as the "Phase-balance equation". Using (5), (9) and (10), oscillation frequency, f_{osc} is given by

$$f_{osc} = \frac{1}{2\pi}\sqrt{\frac{\omega_c R}{L\left(1+\omega_c RC_{eff}\right)}} \tag{11}$$

For this design, f_{osc} is calculated to be 1.154 GHz, ignoring the added capacitors of the tuning systems. Simulation predicts this to be 1.126 GHz. The tuning capacitors with their parasitics will add to C_3 and with the tuning switched off, simulation predicts f_{osc} to be 948.5 GHz where θ_t is about 48º. The digital tuning system is then used to tune it to the ISM band.

B. Criteria for Oscillation

A small-signal equivalent circuit of the oscillator core is shown in Fig. 7. The gain block represents the A-cell and the voltage-dependent current source represents the G_m-cell, where g_m is summation of g_m's of M_3 and M_4. For simplification of analysis, small-signal output resistance, r_o of M_3 and M_4 is ignored.

The relationship between $i_{o,Gm}$ and v_t is given by (8) and $i_{o,Gm}$ is given by the following equation.

$$i_{o,Gm} = -Av_t g_m = \frac{|A|}{1+sT_c}\cdot v_t g_m \tag{12}$$

Here $T_c = 1/\omega_c$. Combining (8) and (12), the following expression is obtained.

$$\frac{|A|}{1+sT_c}\cdot v_t g_m \cdot \frac{R\left\|sL\right\|1/sC_3}{1+\frac{C_2}{C_1}+sC_1\left(R\left\|sL\right\|1/sC_3\right)} = v_t \tag{13}$$

Assuming oscillation has begun, $v_t \neq 0$ and simplifying (13) leads to

$$\begin{aligned} &s^3T_cLRC_{eff} + s^2L\left(T_c + RC_{eff}\right) + \\ &\quad s\left[L + RT_c - |A|g_mLR\left(\frac{C_2}{C_1+C_2}\right)\right] + R = 0 \end{aligned} \tag{14}$$

Equation (14) is the characteristic equation of the proposed GB-LC VCO. Using $s = j\omega$ and then rearranging the real and imaginary terms of the equation leads to

$$\begin{aligned} &R - \omega^2 L\left(T_c + RC_{eff}\right) + j[\omega\{L\left(T_c + RC_{eff}\right) - \\ &\quad |A|g_mLR\left(\frac{C_2}{C_1+C_2}\right)\} - \omega^3 T_cLRC_{eff}] = 0 \end{aligned} \tag{15}$$

Equating the real part of (15) to zero yields

$$\omega^2 = \frac{R}{L\left(T_c + RC_{eff}\right)} \tag{16}$$

Equation (16) gives the frequency of oscillation which is same as (11).

Equating the imaginary part of (15) to zero and using (16), the condition for steady-state oscillation is derived.

$$g_m R = \left(1+\left(\frac{f}{f_c}\right)^2\right)\left(1+\frac{C_1}{C_2}\right)\frac{1}{|A|} \tag{17}$$

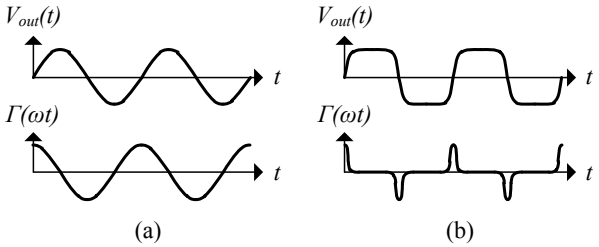

Fig. 8. Waveforms and Impulse Sensitivity Functions (ISF) of (a) a typical LC oscillator and (b) a typical ring oscillator [3].

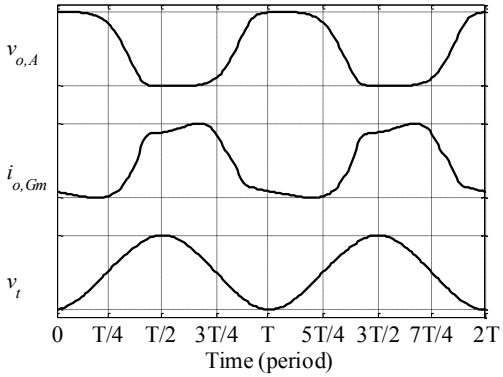

Fig. 9. Normalized waveforms of the proposed GB-LC oscillator.

Initially, for oscillation to start and grow, g_mR needs to be greater than the right-hand side of (17). The following observations can be made from (17):

1) g_m required is increased by the ratio of C_1 and C_2. If C_2 is chosen much larger than C_1, as in this design, this leaves g_m unaffected.
2) g_m required can be reduced in proportion with increase in $|A|$.
3) g_m is also influenced by the high corner frequency of A-cell. The larger the bandwidth, f_c, is than oscillation frequency, the lower g_m is required.

The second and third observations show how power consumption is reduced in the proposed GB-LC VCO. For example, if A-cell is designed with a $|A| = 10$ and $f_c = f_{osc}$, g_m required is 5 times lower than what would be required without the A-cell, thus allowing a much lower startup power than conventional LC oscillators. However, the A-cell would also require significant power. This is where total power consumption of the VCO can be optimized. A-cell has a much smaller load capacitance than the G_m-cell driving the LC-tank and its output resistance and gain are determined by its bias current. Thus, a large f_c can be achieved for A-cell. With high power, A-cell may have f_c much higher than f_{osc} and its phase delay, θ_A would be very small and thus f_{osc} would be very close to tank resonance where frequency sensitivity to device and supply noises are the least.. In this case, the proposed oscillator would have same noise tolerance as a conventional LC oscillator. This is shown in shown in Fig. 3 where the GB-LC curve coincides with the Colpitts curve. Trading off noise tolerance for lower power consumption, f_c can be chosen close to desired f_{osc} while θ_A is small enough for f_{osc} to still remain in the steep portion of the tank-phase curve, achieving acceptable noise tolerance. Thus total power consumption can be

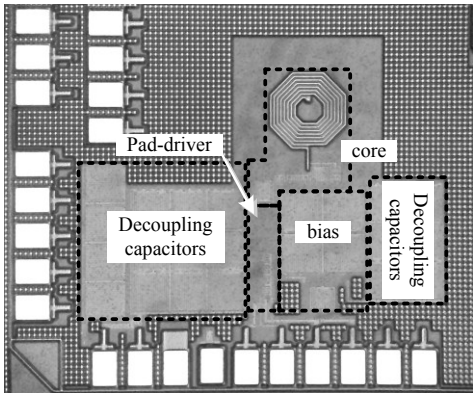

Fig. 10. Microphotograph of the fabricated GB-LC VCO in a bare die. The core occupies 360 µm × 340 µm chip are. Total area including the pads and decoupling capacitors occupy 1.22 mm^2 area.

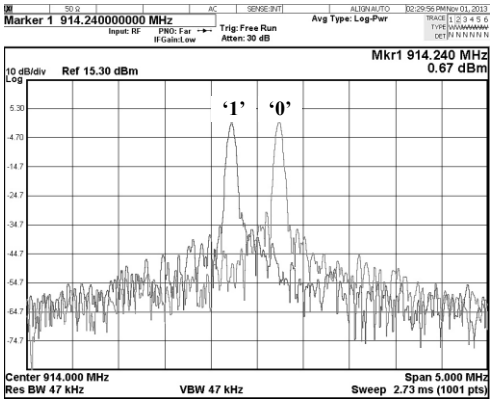

Fig. 11. Measured output spectra of the proposed 2-FSK GB-LC VCO which show about 550 kHz frequency shift around 914.5 MHz center frequency.

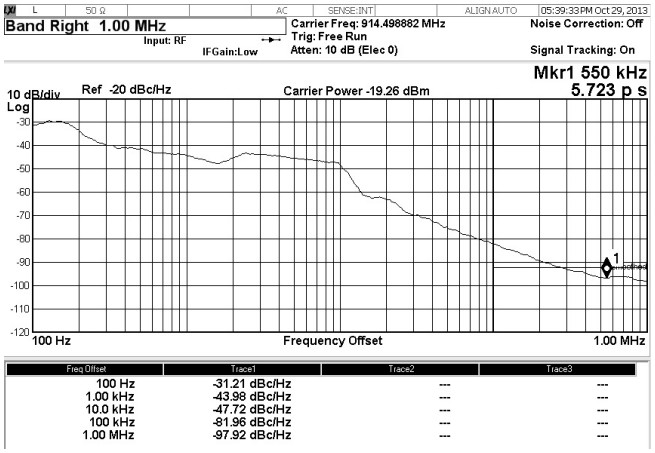

Fig. 12. Phase noise spectrum of proposed GB-LC VCO output tuned to 914.5 MHz. Phase noise is -97.9 dBc/Hz at 1 MHz offset and rms jitter is 5.723 ps measured over 100 kHz – 1 MHz bandwidth.

optimized to be much lower than conventional LC oscillators with sufficiently low phase noise and supply sensitivity.

C. *Phase Noise*

It is known that one of the reasons LC oscillators have generally better phase noise performance than ring oscillators is that in a ring oscillator, charge injections in a node occur during transitions of the driving delay cell [3]. This is when device noise is at a maximum and also when the sensitivity is highest as shown by the Impulse Sensitivity Function (ISF) in Fig. 8. In case of the LC oscillators, charge injection to the tank occurs at

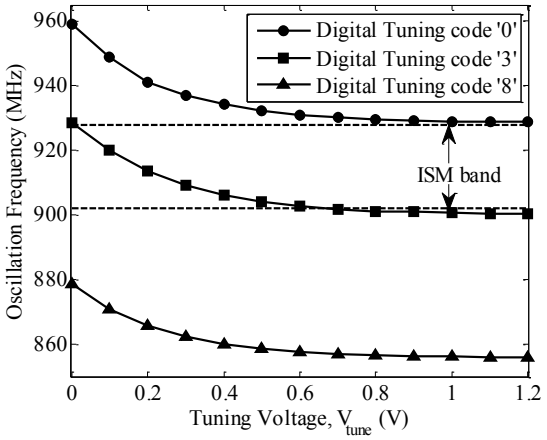

Fig. 13. Tuning range of the proposed VCO. The digital tuning system has a range of 80 MHz which is sufficient to cover for process variations and the analog tuning range varies from 22.5 MHz to 30.2 MHz, corresponding to digital tuning code '0' to code '8'.

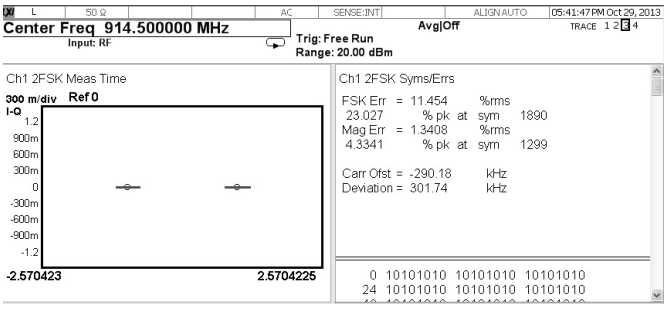

Fig. 14. Constellation diagram and FSK error results of the proposed VCO output. The oscillator is tuned to 914.5 MHz and is 2-FSK modulated with a 100 kHz, 50% square wave simulating '01010101' bitstream at 200 kbps rate. RMS FSK error is about 11.5%.

or near the voltage peak where the ISF is the lowest. As a result, device noise has a much smaller effect than in ring oscillators.

The proposed GB-LC oscillator's normalized waveforms are shown in Fig. 9. The G_m-cell, driven by the almost square waveform output of A-cell, injects charge ($i_{o,Gm}$) into the LC tank and this injection is spread across a wide time-length around tank voltage (v_t) peak instead of in the form of a narrow pulse at the peak that is usual in LC oscillators. This means charge injection is occurring at times other than that which minimizes ISF. As a result, phase noise is degraded in this oscillator structure compared to LC oscillator. Compared to the ring oscillators (where the full 360˚ phase shift around the loop is contributed by noise-sensitive delay cells), in this hybrid oscillator, about 40-50˚ extra phase delay is provided by the single delay cell, which is corrected by the G_m-cell-tank to have a 0˚ or 360˚ around the loop. As a result, oscillation frequency is less prone to delay-cell noise in this hybrid structure.

IV. Measurement Results

The proposed GB-LC oscillator was implemented in a 0.13 µm 1P8M CMOS process. Fig. 10 shows the microphotograph of the fabricated oscillator. The oscillator, including the bias circuits and an additional pad-driver digital buffer needed only for testing purposes, occupies about 700 µm × 340 µm. Included in that area, the core structure with its digitizing output buffer occupies about 360 µm × 340 µm. The

TABLE II
PERFORMANCE COMPARISON WITH EXISTING WORKS

Works	Topology	Process	Frequency	Power consumption	Phase noise (dBc/Hz)	FOM
[4]	Ring	0.35 µm	1.2 GHz	7.01 mW	-90 @ 100 kHz	163.1
[5]	Ring	0.5 µm	900 MHz	15.5 mW	-106 @ 600 kHz	157.6
[9]	Ring	0.6 µm	900 MHz	30 mW	-117 @ 600 kHz	165.8
[10]	Ring	0.13 µm	7.64 GHz	60 mW	-103.4 @ 1 MHz	163.2
[11]	Ring	65 nm	685 MHz	10 mW	-110.8 @ 1 MHz	157
[1]	LC	0.18 µm	403.5 MHz	300 µW	-118 @ 1 MHz	175.3
[12]	LC	90 nm	915 MHz	380 µW	-117 @ 1 MHz	180.4
[13]	LC	90 nm	5.63 GHz	14 mW	-108.5 @ 1 MHz	172
[14]	LC	0.18 µm	900 MHz	4.5 mW	-126.1 @ 1 MHz	178.7
This work	**GB-LC**	**0.13 µm**	**914.5 MHz**	**166.8 µW** **100.1 µW (core)**	**-97.9 @ 1 MHz**	**164.9**

total chip area occupied by the VCO, decoupling capacitors and pads is about 1.22 mm^2. The measurements are performed with an Agilent N9010A EXA signal analyzer.

Fig. 11 shows the output spectrum of the proposed hybrid oscillator operating at 914 MHz frequency. The plot contains two spectra with one binary FSK input at two logic levels. The measured frequency shift is 550 kHz. The FSK system provides two more optional FSK inputs to be used together to obtain larger frequency shifts. With all three FSK inputs tied together, the FSK shift is increased to 1.825 MHz.

The phase noise spectrum with the VCO tuned to 914.24 MHz is shown in Fig. 12. At 1 MHz, phase noise is measured to be -97.9 dBc/Hz. RMS jitter measured over the bandwidth 100 kHz – 1 MHz is 5.723 ps.

Fig. 13 shows the tuning range of the two tuning systems included in the proposed VCO design. The digital tuning range is measured to be 80 MHz, which is sufficient to allow for process variations. The analog tuning range varies from 22.5 to 30.2 MHz and with digital tuning code set to '3', covers the entire 902 – 928 MHz ISM band. The analog tuning is nonlinear and its sensitivity is highest when $V_{tune} = 0$. V_{tune} can be varied within 0 – 0.4 V for an approximately linear analog tuning.

Fig. 14 shows the constellation diagram and error statistics of FSK-modulated output of the hybrid oscillator. The oscillator is modulated with a 100 kHz, 50% duty cycle square wave which simulates a '01010101' bitstream at 200 kbps rate. The selected frequency shift is 550 kHz. The two clusters for two bits in the constellation diagram are well separated and rms FSK error is about 11.5% which is adequate for most low-cost wireless applications [7]. BER can be predicted from this data by calculating the probability of a random variable from a Gaussian distribution, with 0 mean and 11.5% standard deviation, to be greater than 0.5. Thus BER is calculated to be 6.87 ppm.

TABLE I
PERFORMANCE SUMMARY OF THIS WORK

Technology	0.13 µm 1P8M CMOS process
Silicon area	0.24 mm^2 (core, bias, pad-driver)
	1.22 mm^2 (total area inc. pads)
Operating frequency	914.5 MHz
Digital tuning range	80 MHz
Analog tuning range	30.2 MHz (digital tuning at min.)
	22.5 MHz (digital tuning at max.)
Power consumption	166.8 µW *
Supply voltage	1.2 V
Phase noise	-97.9 dBc/Hz @ 1 MHz offset
FOM	164.9
Modulation system	2-FSK (min. 550 kHz shift, 11.5% rms error @ 200 kbps)

* Core power 100.1 µW, excluding digitizing buffer, estimated from simulation. Both figures exclude pad-driver.

The proposed GB-LC oscillator, along with its digitizing output buffer, consumes 166.8 µW from a 1.2 V power supply, when tuned to 914.5 MHz. This excludes power consumed by the additional pad-driver buffer. The digitizing output buffer consumes about 40% of the total 166.8 µW power, as predicted by post-layout simulation. Minimum startup current is measured to be 100 µA.

Figure-of-Merit (FOM) of this hybrid oscillator is calculated using the following equation [8].

$$FOM = -L(\Delta f) + 20\log\left(\frac{f_o}{\Delta f}\right) - 10\log P \qquad (18)$$

Here $L(\Delta f)$ is phase noise in dBc/Hz at Δf offset from oscillation frequency f_o with power consumption of P mW. Thus FOM is calculated to be 164.9. Table I shows comparison of this oscillator to some existing works. The FOM achieved in this work is somewhat inferior to the LC oscillators, and comparable to ring oscillators in Table I, but with lower power consumption than other published oscillators at this frequency. This work is motivated by the need of an ultra-low-power oscillator. Whereas the conventional LC oscillators are hard-limited in case of power consumption reduction because of their startup criteria and the ring oscillators require higher power to achieve phase noise performance comparable to LC oscillators, this hybrid LC VCO topology allows low-power operation with phase noise adequately low for simple low-data-rate systems.

V. CONCLUSION

We have described a novel gain-boosted LC VCO topology that provides designers an intermediate option between the high startup power required by LC VCOs and the poor stability

of ring oscillators. Mathematical analysis for oscillation frequency and startup criteria is presented along with a qualitative comparison of phase noise with conventional oscillator topologies. A summary of measured performance is given in Table II. The designed VCO in this work operates at a center frequency of 914.5 MHz at only 166.8 μW with -97.9 dBc/Hz at 1 MHz offset. The VCO can be tuned across 80 MHz with a 4-bit digital control and at least 22.5 MHz with rail-to-rail analog tuning. The VCO is implemented with a 2-FSK system with 550 kHz shift that shows only 11.5% rms error at 200 kbps, sufficient for BER < 100 ppm. The novel hybrid topology allows reduction of the startup power compared to LC oscillators and thus allows ultra-low-power operation with phase noise adequately low for simple low-data-rate communication systems.

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