A Micro-Power Neural Spike Detector and Feature Extractor in .13µm CMOS

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***Abstract*— We present a fully-integrated system for the detection and characterization of action potentials observed in extracellular neural recordings. The circuit includes an analog implementation of the nonlinear energy operator for spike detection. The minimum and maximum value of detected spikes are captured by peak detectors and digitized by an on-chip successive approximation ADC to provide a compact description of the spike waveform. The circuit is implemented in a .13 µm CMOS process. It occupies .17 mm^2 of chip area and consumes 1 µW from a 1 V supply.**

I. Introduction

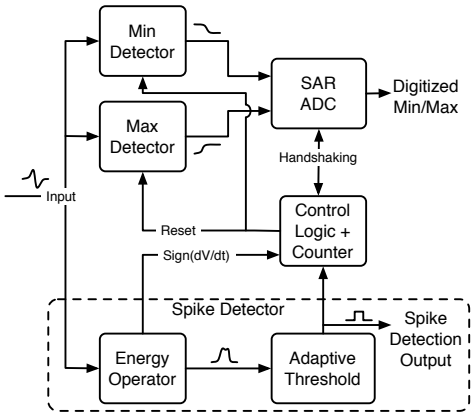
Many neural recording applications focus on action potentials, spikes generated by individual neurons. Action potentials occupy the frequency range roughly between 100 Hz and 5 kHz, and occur at a rate up to about 100 per second. Adequate digitization would require a neural signal to be sampled at 10 kS/s, even though around 90% of the digitized samples would not be part of an action potential. These "empty" samples must be processed using local computer cycles or transmitted via a wireless link for off-chip processing. Either choice results in unnecessary power dissipation and would be prohibitive for an implanted multi-channel system. Additionally, measurement of non-linear features such as spike amplitude and width requires that the signal be either oversampled or digitally interpolated, further increasing demands on the analog-digital converter (ADC) or local processor.

In this paper we present a circuit to perform spike detection in the analog domain, precluding the need to digitize the entire waveform. After a spike is detected, the maximum and minimum values are digitized with an 8-bit successive approximation ADC. By extracting the most important features of the signal in the analog domain, the power required to digitize the entire waveform is greatly reduced. Compared to a simple thresholding scheme, our architecture provides additional information by capturing the maximum and minimum values of the action potentials, which can be used for further processing, including spike sorting. Additionally, the nonlinear energy operator (NEO), which we use to implement our spike detector, has superior discriminatory ability to a threshold-based detector.

II. System Design

A. Architecture

The neural interface circuit, shown in Fig. 1(a), comprises a spike detector for distinguishing action potentials from noise, positive and negative peak detectors to characterize the detected spike, and an ADC to digitize the spike maximum and minimum. The proposed circuit is intended to follow a pre-amplifier that amplifies the neural signal to an amplitude of approximately 400mV peak-peak. The spike detector is the first component in the signal chain. When a spike is detected, a counter is triggered to provide a delay equal to twice the width of the spike. The delay ensures that the maximum and minimum occur and are captured before the ADC is triggered. After the delay has elapsed, the "Ready" signal is asserted, which causes the ADC to digitize the captured minimum and maximum values. The digitized values are then read through a serial interface. After both conversions are complete, the ADC asserts the "Done" signal, which triggers a reset of the peak detectors and control logic, preparing the system for the next spike detection.



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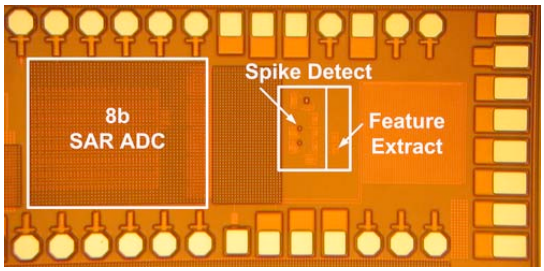


(b)

Fig. 1. (a) System architecture. (b) Die photo.

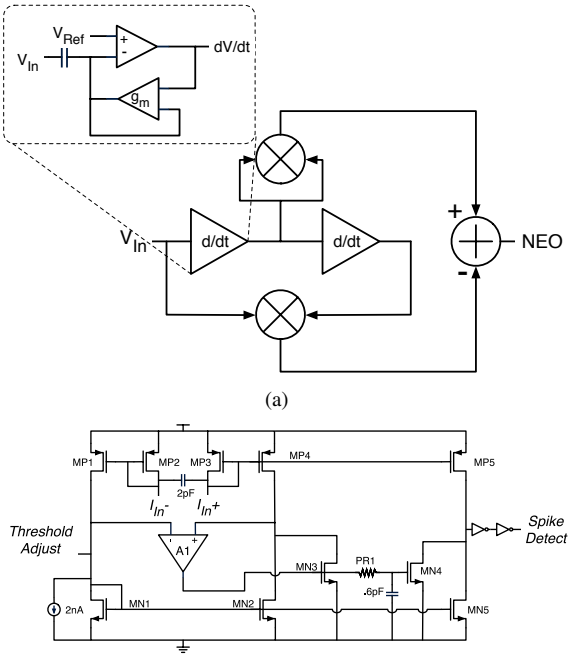


Fig. 2. Spike detector. (a) Nonlinear energy operator. (b) Adaptive threshold circuit. The NEO output in (a) is a differential current which is is the input to the thresholding circuit in (b).

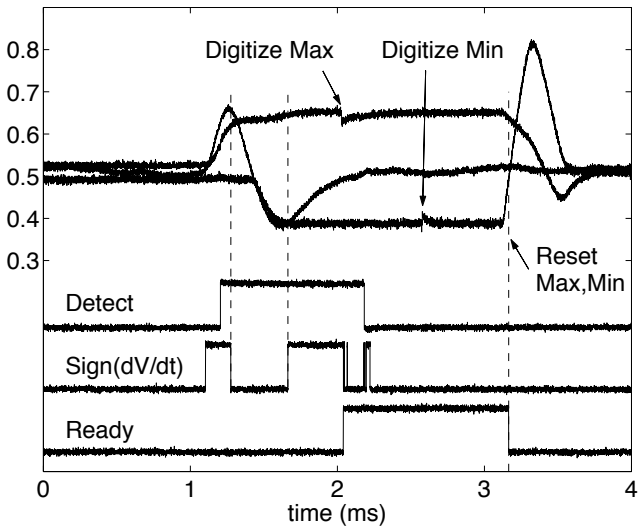


Fig. 3. Spike detection timing. Input, V_{Max}, and V_{Min} are shown at the top, followed by the digital timing signals involved in the detection sequence.

The detection sequence is shown in Fig. 3. The first two edges of sign(dV/dt) after the spike detection, marked with dashed lines, indicate the time of the positive and negative peaks. The time between the two edges is the measured spike width. The rising edge of Ready initiates the A/D conversion. A handshaking signal from the ADC (not shown) indicates that the conversion is complete and resets the peak detectors and timing logic, marked by the third dashed line.

B. Spike Detector

A schematic of the spike detector is shown in Fig. 2. An analog implementation of the nonlinear energy operator (NEO) provides a differential output current which indicates the amount of activity in the input signal. The nonlinear energy operator (NEO), defined as

$$NEO(x) = \dot{x}^2 - \ddot{x}x,$$

has been found to discriminate between spikes and noise better than a simple thresholding detector, particularly when the signal-noise ratio (SNR) is low [1]. The spike detection operation is traditionally performed offline using a PC.

The two differentiations are performed by g_m-C differentiators. The multiplications are performed by Gilbert cells. The differential current outputs are connected to perform the subtraction. The multiplier inputs are differential, with the positive inputs taken from the single-ended outputs of the differentiators. The DC levels of the positive multiplier inputs are computed by low-pass filters (not shown) using a pseudo-resistor realized from anti-parallel diodes [2] and connected to the negative multiplier inputs. This arrangement, made possible because there is no useful DC information in any of the signals, prevents offsets in the differentiators from corrupting the NEO output.

The adaptive thresholding circuit shown in Fig. 2(b) converts the NEO output into a binary spike detection signal. Any activity in the input signal, including noise, will result in a positive NEO output. In order to minimize false detections, the threshold must be set above the background noise level. The feedback loop formed by A1 and MN3 sets $I_{D,MN3}$ equal to the differential NEO input current. This quantity is then low-pass filtered and doubled through the current mirror formed by MN3 and MN4. The low-pass corner frequency is set to around 1-2 Hz by realizing PR1 as a pseudo-resistor formed from anti-parallel diodes. Thus the NEO input required to cause a detection is set at twice the average background activity. The current source in parallel with MN1 ensures that current is flowing through MN3 even when the differential input is zero. A threshold adjustment current can be injected to vary the sensitivity of the spike detector. The current mirrors in the thresholding circuit all have cascodes, which are omitted from the figure for clarity. Because the current mode signaling allows for small voltage swings, cascodes are possible even with a supply voltage of 1V.

C. Feature Extraction

Positive and negative peak detectors capture the extreme values of the signal. The positive peak detector is shown in Fig.4, and the negative detector uses the same topology with opposite polarity. The use of a differential pair to charge the storage capacitor allows $V_{SG,MP1}$ to be made less than 0 V, minimizing subthreshold current in MP1, which could cause the peak detector output to drift to V_{DD} during periods with little activity. When the Ready signal is issued to the ADC, Hold is simultaneously asserted in the peak detector. The peak detector input is forced to 0 V, preventing the output

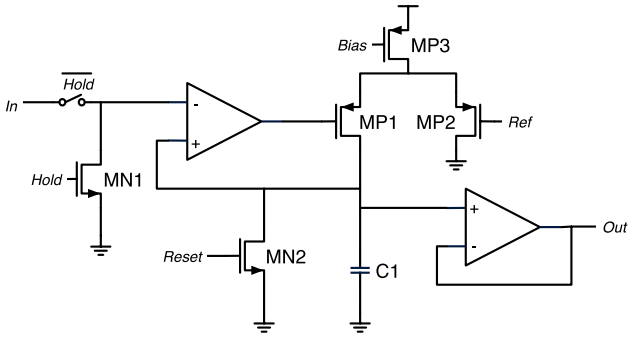


Fig. 4. Peak detector.

from changing during the analog-digital conversion. After the conversion is complete, Hold is released, and Reset briefly forces the output to 0 V.

A digital counter is used in conjunction with the differentiators from the NEO to measure the width of the spike. The first differentiator has an auxiliary sign output. A change in the sign of the first derivative indicates a minimum or maximum in the input signal. After a spike is detected, the next change in the derivative sign starts the counter. The second change in the sign output causes the counter value to be registered for readout and the counter to count back down to zero. The additional delay allows time for the extreme values of the spike occur and be sampled by the peak detectors. When the counter returns to 0, the Ready signal is asserted to initiate conversions of the maximum and minimum voltages. The counter is also intended to provide a measurement of the spike width, defined as the time between the maximum and minimum of the spike.

D. Analog-Digital Converter

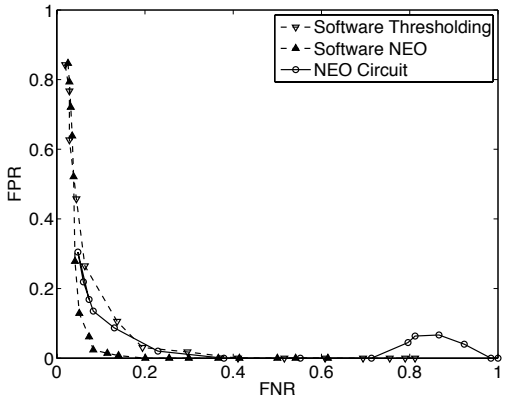
The 8-bit ADC was designed to operate from 10 kS/s to 100 kS/s. A successive approximation register (SAR) architecture was chosen for the ADC to minimize power consumption [3][4]. The digital ADC output is read serially from the comparator output. A synchronization signal, which is used internally to purge the DAC capacitor array and SAR logic after each conversion, also synchronizes the serial output.

III. RESULTS

The system was implemented in a .13µm CMOS process. The spike detector and feature extractor occupy a die area of 200µm x 220µm. The ADC occupies 295µm x 430µm, of which about 85% is consumed by the DAC capacitors.

The ADC is functional for sampling frequencies from 100 S/s to 1MS/s. At a 1.2 V power supply, with the positive and negative reference voltages taken from the supplies, and -0.25 dBFS input, SNDR=39.23 dB, and SFDR=46.5 dB, leading to an ENOB of 6.22 bits. The non-ideal ENOB arises from time-varying noise as well as non-linearity. The worst DNL is 0.31 LSBs. The worst INL is 1.42 LSBs.

To test the sensitivity of the spike detector, we used an artificial neural recording [5]. An artificial recording allowed variation of the noise level and spike rate, and provided a ground truth reference against which to compare spike detector accuracy. With an actual recording, there is no guaranteed correct reference, since a neural recording is subject to differences in interpretation, even among expert neurophysiologists [6].



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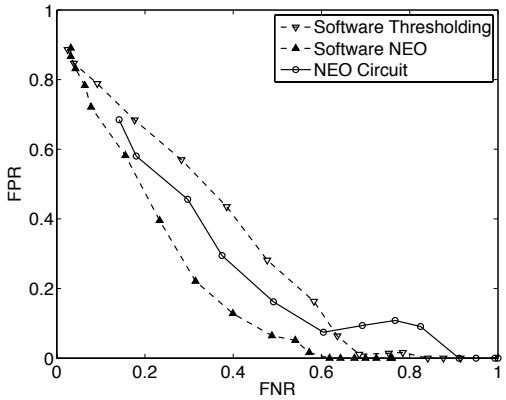
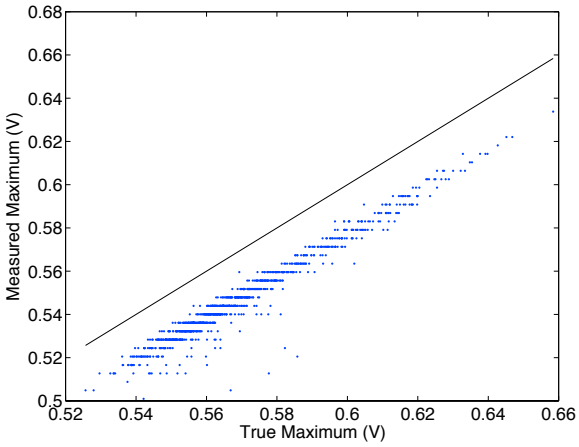


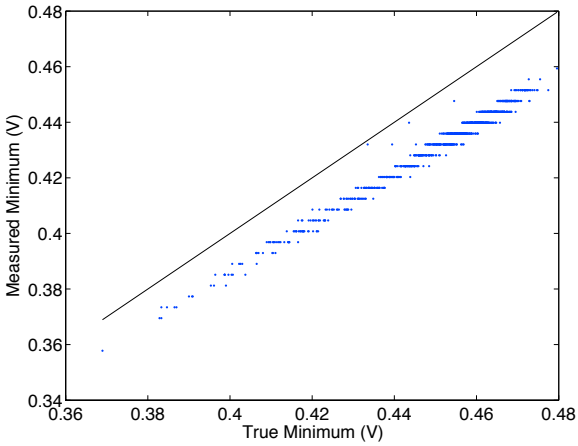
(b)

Fig. 5. False positive rate (FPR) versus false negative rate (FNR) for the threshold-based software spike detector, the proposed analog NEO detector, and a software implementation of the NEO operator. FPR = False detections / Total detections. FNR = Undetected spikes / Total true spikes. (a) SNR=10 dB. (b) SNR=6 dB.

Spike detections from the circuit were compared with labels from the generating software to determine the sensitivity and selectivity. For comparison, we also applied a threshold-based software spike detector to the same signal. The software detector indicated a spike whenever the absolute value of the input exceeded a specified threshold. We tested both detectors with several different threshold values to build the curves shown in Fig. 5. The y axis shows the false positive rate (FPR), the fraction of detections determined to be false. The x axis shows the false negative rate (FNR), the fraction of true spikes that were not detected. With a 10 dB SNR, shown in Fig. 5(a), the threshold-based software detector has good discriminative abilities. Fig. 5(b) shows the same curves measured with an SNR of 6 dB. With the noisier signal, the discriminative power of the NEO yields a superior detector at most threshold levels.



(a)



(b)

Fig. 6. Accuracy for capture and digitization of the spike maximum and minimum values. The solid lines indicate equality of true and measured values.

A digital counter is included to measure the width of the spike, defined as the time elapsed between the positive and negative peaks. However, due to variation in the relative timing between the rising edge of the detection signal and the first peak of the spike, the timing measurement is not reliable.

To test the accuracy of the peak detection and digitization, we simultaneously recorded the digital output of the ADC, the timing signals, and the input waveform. We then compared the ADC output to the actual minimum or maximum value that should have been digitized. The comparisons are shown in Fig. 6. At the end of each pair of conversions, the ADC handshaking signal resets the two peak detectors to allow a new peak to be captured. The true value, plotted on the x axis, is computed from the recorded input signal as the maximum or minimum value in the time interval between the beginning of a given digitization and the end of the last digitization. The results shown in Fig. 6 are for spikes detected when at least 2 ms has occurred since the most recent conversion-reset cycle. For applications such as spike sorting, deterministic errors

TABLE I

PERFORMANCE SUMMARY

Process	.13 μm CMOS
Active Area	.17 mm^2
V_{DD}	1.0 V
Power	.95 μW

such as gain error and offset are less important than random variations due to noise. Offsets due to the peak-detecting circuits have been subtracted based on a DC measurement. The remaining offset is due to the ADC. The RMS error relative to a linear fit is 4.5 mV (1.2 LSB) and 2.0 mV (0.5 LSB) for the maximum and minimum, respectively.

Previous work which has implemented similar processing entirely in the digital domain [7], consumed approximately 1 μW/channel to perform spike detection and calculate the maximum, minimum, and width of detected spikes, in addition to the power required for the ADC.

IV. CONCLUSION

We have presented a low-power circuit which performs detection and feature extraction on extra-cellular neural signals. Our system demonstrates that complex digital logic can be replaced by compact low-power analog circuits. By performing simple computation in the analog domain, demands on analog-digital conversion and on local processing or communications bandwidth are reduced, enabling a reduction in overall system power.

The proposed system can easily be extended to multiple channels. Simple digital multiplexing would allow the ADC, the most area-intensive component, to be shared by many channels. By greatly reducing the required conversion rate, the analog processing we have described also facilitates the sharing of one ADC among many channels.

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