A Compact Pulse-Based Charge Pump in 0.13μm CMOS

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***Abstract*— In this paper, we present a new class of charge pump capable of generating voltages 3.75 times greater than the supply in a single clock cycle. It occupies .005 mm^2 in a 0.13μm CMOS process and can operate with a supply voltage between 0.4V and 1.2V, or as low as 0.2V with some pulse-shape distortion. Our charge pump can provide output voltages of up to 3.9V with less than 10nW of standby power dissipation.**

I. Introduction

The emergence of wireless sensor networks has driven a growing demand for circuits that can operate with very low supply voltages. Sensors may be required to operate from a single cell or from harvested energy sources, resulting in an available supply of 0.4V-1.5V. Some technologies require a higher bias voltage, and in these cases, charge pumps can provide a voltage larger than the positive supply. For example, micromechanical (MEMS) resonators [1] require a high bias voltage (2.5V-10V) to reduce their motional resistance, but do not draw current from the high voltage supply. A charge pump with very fast turn-on and turn-off times could be used to enable a MEMS-based oscillator or filter bank for short-burst communication. Non-volatile memories based on floating gates have been demonstrated to enable extremely power-efficient computation [2]. High voltages are needed to induce Fowler-Nordheim tunneling for programming floating-gate memories, but negligible current is consumed. Boost converters present another application for for a pulse-based charge pump. During sustained operation, a boost converter can use its own high-voltage output to supply the control circuitry, but during startup, a sufficiently high voltage must be supplied externally. For example, experimentation has shown that a TI TPS61001 requires 0.8V initially, but can operate from 0.3V after the output has reached 0.8V, if the control logic is powered by the output. A circuit able to deliver a brief, high-voltage pulse from a low supply would allow the boost converter to be bootstrapped from a supply below its nominal startup requirements.

Previously presented charge pumps, such as [3], use a clock to gradually accumulate charge, generating a sustained high voltage. For circuits that only require a brief, occasional pulse at a high voltage, the power required to continuously operate a charge pump over a long interval could be saved if it were possible to generate and remove a high voltage in a single pulse. In this paper, we present a charge pump which generates a high-voltage from a single pulse of a digital control signal. Our charge pump does not suffer any device threshold or diode drops, because the charge flow is controlled by MOS switches rather than diodes. It also does not require an oscillator, allowing for simple system design and low area overhead. The charge pump operates from a supply between 0.4V and 1.2V. The core functionality is maintained at a supply of 0.2V, although the turn-off characteristic is poorly defined because of weak conduction in switches to ground. These attributes make our charge pump attractive for low-power, low-voltage applications.

II. Circuit Design

Our charge pump comprises five stages, as shown in Fig. 1(a). When the Enable input is 0, S_{VDD}=S_{GND}=1 and S_{CPL}=0, charging each capacitor C_{Pump} to V_{DD}. When Enable is high, S_{VDD}=S_{GND}=0 and S_{CPL}=1, disconnecting the capacitors from V_{DD} and ground and connecting them in series to yield the multiplied output voltage.

On Enable's rising edge, the switching events are ordered such that the stages switch in reverse order, starting at stage 5. Within each stage, the ground switch S_{GND} is opened first, followed after a short non-overlap period by the closing of the inter-stage coupling switch S_{CPL}. S_{VDD} must remain closed long enough for V_{Out} to charge to V_{DD} through S_{CPL}. When any stage k switches, all of the subsequent stages, $k+1$ through 5, have already switched. The pumping capacitors, which are now in series from stage k to the charge pump output, are AC short circuits, so the V_{DD} step applied to the output of stage k must propagate through all of the subsequent coupling switches. The switch resistances combine with the parasitic capacitance C_{Par} at each stage to form an RC chain. The total time constant from the V_{DD} connection of stage k to the charge pump output can be approximated using an Elmore delay model as

$$\tau_k = \sum_{i=1}^{N-k+1} (i+1)R_{Sw}C_{Par} + (N-k+1)R_{Sw}C_{Load}, \quad (1)$$

where N is the total number of stages, in this case five. After S_{CPL} is closed, a fixed delay is provided to allow the

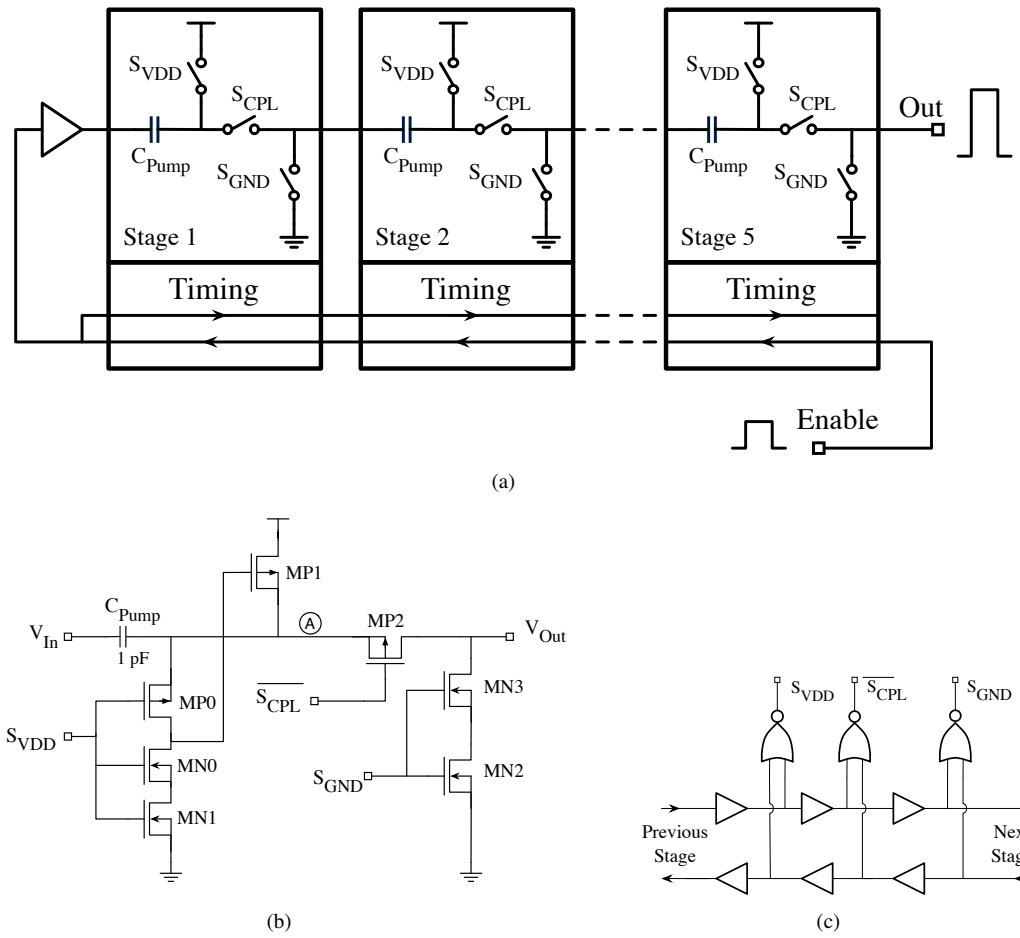

Fig. 1. (a) Architecture of the charge pump. (b) The switching circuitry of a single stage. (c) The timing generation for a single stage.

V_{DD} step to propagate to the charge pump output. Then, S_{VDD} is opened, and the whole process is repeated in the previous stage. When the Enable signal is lowered, the entire process occurs in reverse, starting with the first stage. Correct ordering of the switching events on the falling edge of Enable is necessary to ensure that charge remaining on the capacitors is not lost through a transient short, requiring extra current to be drawn from the supply.

The schematic of a single stage is shown in Fig. 1(b). The charge pump output voltage appears across S_{GND} in the last stage, and leakage through MN2 and MN3 while S_{GND} is open limits the maximum output. Transistor lengths were chosen to avoid drain-source punch-through. To reduce the effect of leakage through the reverse-biased drain-bulk junctions, S_{GND} is implemented using two NFETs in series, MN2 and MN3. We have utilized the deep N-well to connect the bulk terminal of MN3 to its source, so that both drain-source and bulk junction leakage raise the voltage on the shared node between MN2 and MN3, allowing high voltages to be divided between the two NFETs.

S_{VDD} is implemented by MP1. When the charge pump is active, V_A is higher than V_{DD}, so the gate voltage of MP1 must be at least V_A to keep MP1 turned off. The gate of MP1 is controlled by MN0,MN1 and MP0, which act as an inverter supplied by V_A. Node A is always at the highest potential in a given stage, and switches between V_{DD} and a higher voltage, so all PMOS wells are tied to node A. Because MN0 and MN1 are also exposed to the stage output voltage, they are connected in the same arrangement as MN2 and MN3. The coupling switch S_{CPL}, implemented by MP2, conducts during the active phase of the charge pump. The maximum voltage between its source and drain is V_{DD}, so it does not require the leakage reduction techniques used for S_{GND}. The well-substrate junction is exposed to the output voltage, but because of the lower doping levels in the well and substrate, leakage from the well is small compared to other sources of leakage.

The switching events are controlled by a timing circuit in each stage, shown in Fig. 1(c). A chain of delay elements from the last stage to the first stage determines timing on Enable's rising edge, and another delay chain going in the opposite direction determines timing on the falling edge. NOR gates are used to generate the actual switching signals from delayed versions of Enable.

The pumping capacitors were implemented using metal-insulator-metal (MiM) capacitors directly above the active

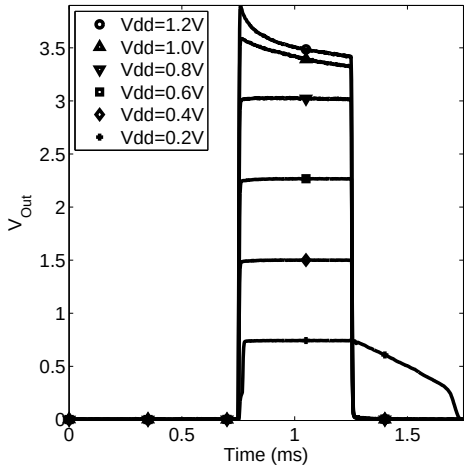

Fig. 2. Charge pump output for several values of V_{DD}.

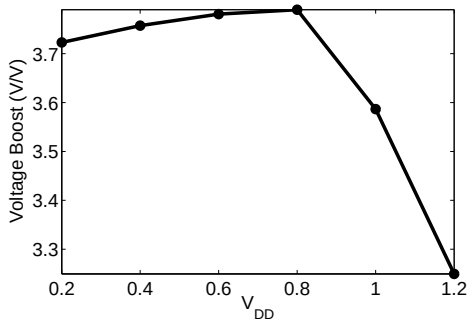

Fig. 3. The voltage multiplication ($V_{Out,Max}/V_{DD}$) as a function of supply voltage.

circuitry to conserve area. We used 3.3V transistors for the switching circuits and 1.2V transistors for the timing.

III. Results

We fabricated the charge pump in a commercially available 0.13µm CMOS process. It occupies $141\mu m \times 35\mu m$ and operates from a single supply of 0.4V-1.2V. A die photograph is shown in Fig. 4. For testing, the output at each stage was buffered with an open-source PMOS follower and measured off-chip.

Fig. 5(a) and (b) show the intermediate voltages at the output of each stage, with V_{DD}=0.4V and 1.2V, respectively. Fig. 5(c) and (d) show the voltage increase associated with each stage at the respective supply voltages. Fig. 5(c) shows that the voltage increases due to the later stages are larger than those due to the earlier stages. Each stage drives the parasitic capacitance of all downstream stages, so the V_{DD} step applied to each stage's output is more attenuated for the earlier stages. With V_{DD}=1.2V, junction leakage limits the voltage increase at the later stages.

Fig. 2 shows the output voltage for several values of V_{DD}. For supply voltages between 0.2 and 0.8 volts, the peak output is between 3.75 and 3.8 times the supply. The voltage multiplication, defined as $\max(V_{Out})/V_{DD}$, is shown as a

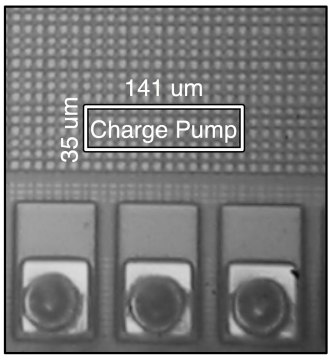

Fig. 4. Chip microphotograph. The active circuitry is obscured by the fill pattern, but three bondpads are included for a scale reference.

function of supply voltage in Fig. 3. For higher voltages, the output begins to plateau due to leakage, corresponding to a lower multiplication factor. According to simulation results, the leakage occurs primarily in the bulk-drain junctions of MN1 and MN2. This leakage is also manifested in the shape of the output pulse. For lower supply voltages, the output stays approximately constant during the 0.5ms pulse. For higher supply voltages, corresponding to output voltages of 3V and higher, the output exhibits a decaying response. With the V_{DD} below 0.4V, the charge pump remains functional, but turns off very slowly. This is due to the increased on resistance of S_{GND}.

Static power consumption is set by subthreshold leakage and varies from 1.63nW when V_{DD}=0.4V to 9.29nW when V_{DD}=1.2V. Simulations indicate that both static and dynamic power consumption are dominated by the timing circuitry. Fig. 7(a) shows the energy consumption per pulse as a function of supply and frequency, for a pulse width of 5µs. Current consumption beyond static leakage is proportional to pulse frequency, and approximately independent of pulse width. As tested, the charge pump is loaded only by the source follower, which presents an approximately 10fF load.

Power efficiency is a common figure-of-merit for charge pumps. However, our charge pump is intended for capacitive loads or other low-current applications, where output power is not a meaningful metric. We will use energy efficiency, the ratio of available energy at the output to dissipated energy per pulse, as our efficiency metric. Energy efficiency is shown in Fig. 7(b). Available energy is computed as $E_{Out} = V_{Out}^2 C_{Load}$, and energy consumption per pulse is computed as $E_{In} = V_{DD} I_{DD} / F_{Pump}$. Because power consumption is dominated by the timing network, energy efficiency would be increased with a larger load capacitance.

Minimum pulse width is determined by the the round-trip propagation delay of the timing circuits, which in turn is limited by the propagation delay through the coupling switches defined in (1). Simulations show that the minimum pulse width is about 25ns with V_{DD}=1V, but the source follower we used to measure the output lacks the bandwidth to directly measure

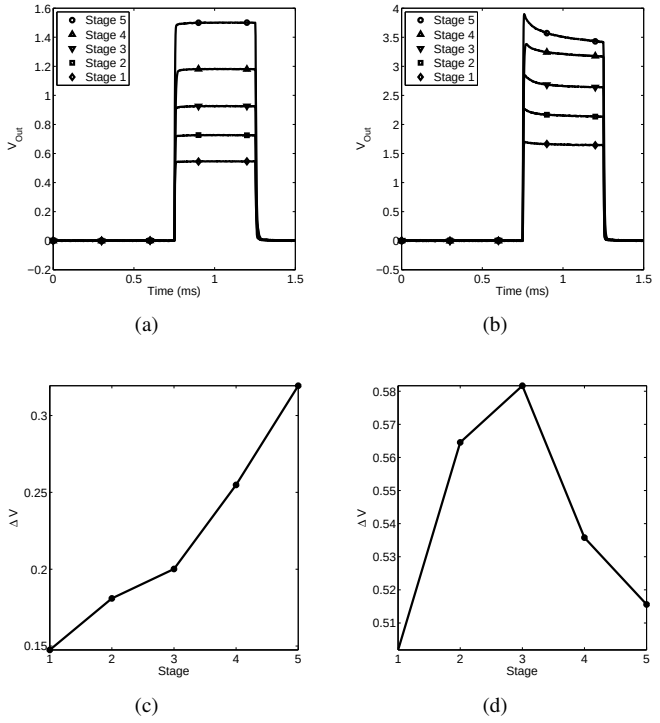

Fig. 5. Output voltage at each tap for Vdd=0.4V (a) and 1.2V (b). The portion of the voltage boost occurring in each stage for V_{DD}=0.4V (c) and 1.2V (d).

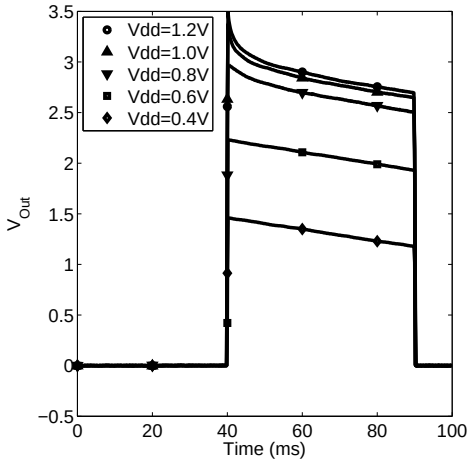

Fig. 6. Charge pump output for a longer (50ms) pulse.

pulses of this width. Maximum pulse width is limited by leakage. Fig. 6 shows the charge pump output for a 50ms pulse at various supply levels. With V_{DD} between 0.4V and 0.8V, the charge pump maintains 90% of its peak output for over 20ms.

IV. Conclusion

We have presented a new class of charge pump circuit which requires only a single pulse from a digital control signal to generate high voltages. Because our charge pump does not require an external oscillator, it enables the generation

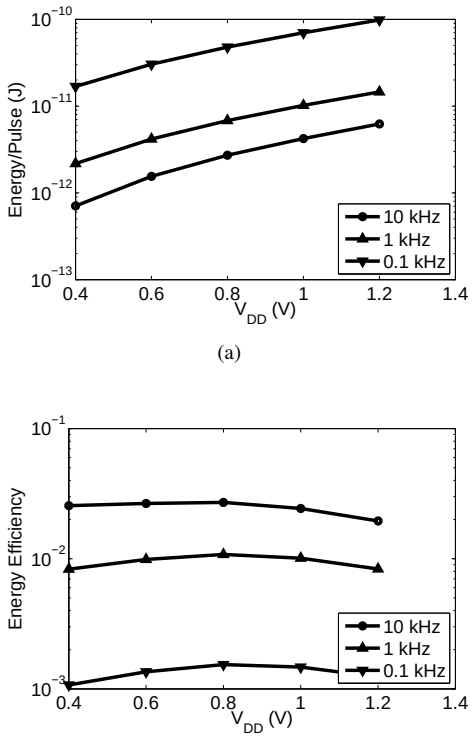

Fig. 7. For three pulse frequencies, (a) the energy dissipated per pulse, and (b) the energy efficiency.

of voltages above the supply with minimal area or power overhead. It operates from supply voltages as low as 0.4V with standby current under 10nW, making it attractive for low-voltage low-power applications that need a high-voltage low-current bias voltage.

TABLE I
PERFORMANCE SUMMARY

V_{DD}	0.4V	1.2V
Voltage Multiplication	3.75	3.25
Energy Efficiency, F=10 kHz	2.56%	1.95%
Static Power Dissipation	1.63nW	9.29nW
Area	.005 mm^2	

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