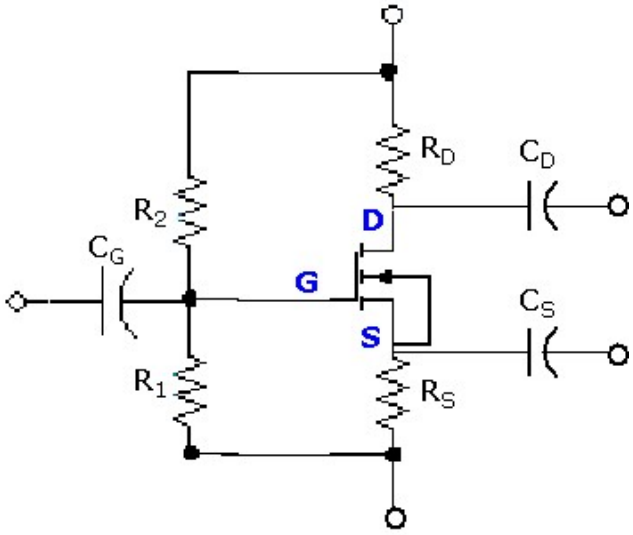
Section J6: FET Amplifiers & Amplifier Analysis

Just as there were four basic configurations for a single stage BJT amplifier (CE, ER, CC, and CB), there are four basic configurations for a single stage FET amplifier. With respect to the figure to the right (a modified version of Figure 6.31 in your text), these configurations may be defined as follows:



- In the **common source (CS)** configuration, the ac input is applied at C_G, the ac output is taken at C_D and C_S is connected to a dc voltage source or ground. This is analogous to the common-emitter configuration of the BJT. Note the distinction between CS (the configuration) and C_S (the capacitor) – don't let this confuse you.
- In the **source resistor (SR)** configuration, the ac input is applied at C_G, the ac output is taken at C_D and C_S is omitted. This is analogous to the emitter-resistor configuration of the BJT.
- In the **common gate (CG)** configuration, the ac input is applied at C_S, the ac output is taken at C_D and C_G is connected to a dc voltage course or ground. Sometimes in the CG configuration, C_G is omitted and the gate is connected directly to a dc voltage source. The CG is analogous to the common base configuration for the BJT, although it is seldom used. Note the distinction between CG (the configuration) and C_G (the capacitor) – don't let this confuse you.
- In the **source follower (SF)** configuration, the ac input is applied at C_G, the ac output is taken at C_S and the drain is either connected to a dc voltage supply (with or without C_D). This is also called the **common drain (CD)** and is analogous to the common collector (a.k.a. emitter follower) configuration for the BJT.

Although the circuit above shows an enhancement NMOS, these configurations are valid for all JFETs and MOSFETs discussed. Also, keep in mind that the circuit capacitors serve as coupling or bypass, depending on the configuration, and are assumed to be large enough to act as open circuits for dc and short circuits for the frequency range of interest.

In the following sections, we will examine each of these configurations in detail. Similar to the BJT amplifier analysis, we will derive equations for the voltage gain, current gain, input resistance and output resistance.

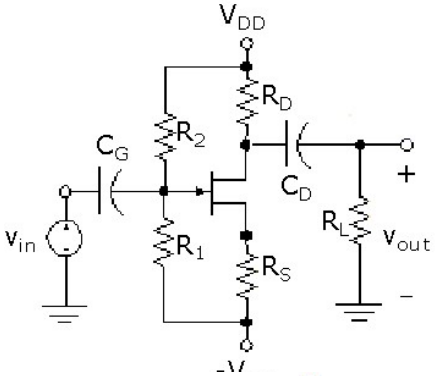
For the 90-gajillionth time,

- ***Always*** keep in mind that the total voltage and current are composed of a dc component and an ac component. For the small-signal model to apply, the transistor must stay in the active (saturation) region for the entire range of input signals. The dc voltages and current that characterize the bias conditions must be defined such that the transistor stays in the active region for all expected input signals.
- Although the figures are shown with purely resistive input and output characteristics, occasions may arise where these parameters are complex values. Don't let this throw you, the process is the same but life gets a little more complicated and we will be dealing with Z_{in} and Z_{out}.
- Don't just grab equations – although the assumptions we're going to make in the following derivations are generally valid, make sure you ***know*** that they are before using the equations!
- The following amplifier circuits are shown using n-channel JFETs. All derivations, equations, etc., are valid for all JFET and MOSFET devices discussed, with appropriate modifications.

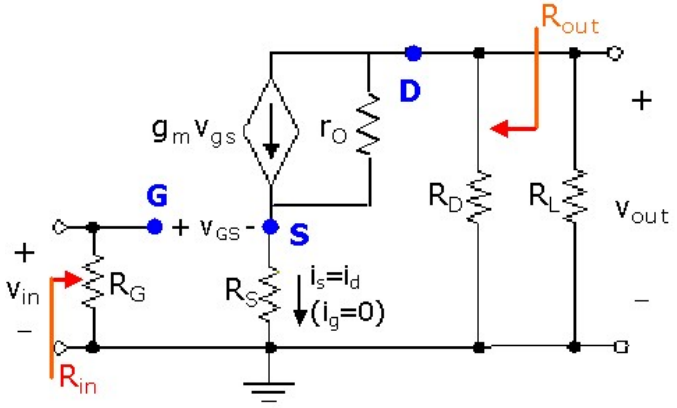
The CS and SR Amplifier

To avoid duplicate derivations, the following discussion will focus on the source resistor configuration. From the source resistor results, we can obtain expressions for the common source configuration by setting $R_S=0$ in all equations (since R_S is bypassed by C_S in the CS configuration).

The SR amplifier circuit is shown to the right (based on Figure 6.33a of your text). As defined above, the ac input is applied at C_G and the ac output is taken at C_D. The CS amplifier circuit is exactly the same with the addition of C_S, which is connected to the dc voltage source or ground.



The ac small signal model for the source resistor configuration is shown to the right and is a modified version of Figure 6.33b in your text. I have explicitly



shown the device output resistance, r_O, in this circuit for the sake of completeness. However, as we found for the BJT (and your author assumes), this output resistance is usually much larger than the resistances it is in parallel with and may be neglected. By following the same strategy as we used for the emitter-resistor configuration, R_{out} for the source resistor configuration is found to be

$$R_{out} = [r_O + R_S(1 + g_m r_O)] \| R_D .$$

Note that if $r_O >> R_S$ and $r_O >> R_D$, this may be simplified to

$$R_{out} \cong R_D .$$

By inspection, the input resistance of the SR circuit is

$$R_{in} = R_G = R_1 \| R_2 .$$

To calculate the voltage gain, we need expressions for v_{in} and v_{out} in terms of circuit components. The following presentation is slightly different from your text's derivation, but we get to the same place.

To solve for v_{in}, we write a KVL equation around the gate loop:

$$v_{in} = v_{gs} + i_d R_S = v_{gs} + g_m v_{gs} R_S = v_{gs}(1 + g_m R_S) . \qquad \text{(Equation 6.42)}$$

The output voltage may be expressed as

$$v_{out} = -i_d (R_D \| R_L) = -g_m v_{gs} (R_D \| R_L) .$$

Calculating the voltage gain $A_V = v_{out}/v_{in}$, we get

$$A_V = \frac{-g_m (R_D \| R_L)}{(1 + g_m R_S)} = \frac{-(R_D \| R_L)}{R_S + 1/g_m} . \qquad \text{(Equation 6.43)}$$

Finally, either by using the gain impedance formula or by using a current divider to define the output current (the current through the load) and defining current gain in the usual way, we get

$$A_i = \frac{-R_G}{R_S + 1/g_m} \frac{R_D}{R_D + R_L} . \qquad \text{(Equation 6.45)}$$

As mentioned earlier, the relevant equations for the CS configuration may be found by modifying what we've just derived. Specifically, when $R_S=0$, the common source configuration results are:

$$R_{out} = r_O \,||\, R_D \cong R_D \quad if \quad r_O >> R_D$$

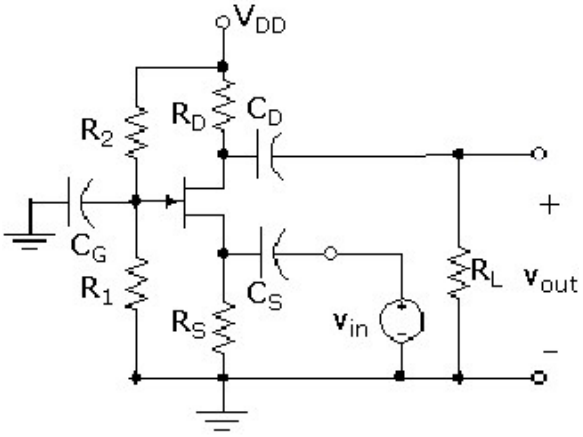
$$R_{in} = R_G = R_1 \,||\, R_2$$

$$A_V = -g_m (R_D \,||\, R_L)$$

$$A_i = \frac{-g_m R_G R_D}{R_D + R_L}$$

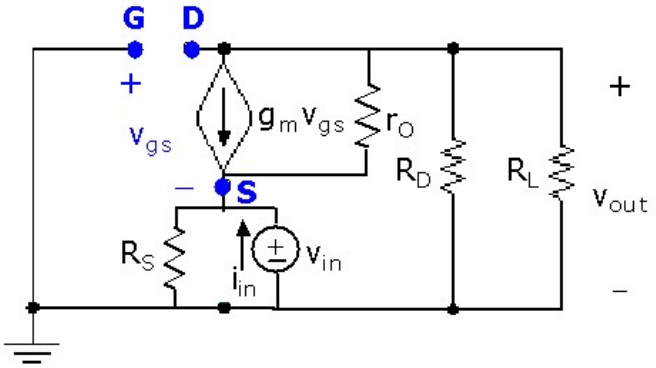
Finally, note that the voltage and current gains for both the CS and SR configurations are negative, indicating a 180° phase shift between input and output (just like we had for the BJT CE and ER).

The CG Amplifier



A modified version of Figure 6.37a is shown to the right. *In this schematic of a common gate amplifier, I have removed the source resistance R_{source} and applied v_{in} directly. What I'm trying to do here folks is maintain consistency in the notation – when we use v_{in} it is applied directly to the amplifier. An alternate representation is the derivation of v_{in} through a voltage divider relationship from a source voltage and resistance (v_{source} and R_{source}).* As defined in the introductory comments of this section, the ac input is applied at C_S, the ac output is taken at C_D and C_G is connected to ground.

The ac small signal model for the CG amplifier is shown to the right (Note that the illustration given in Figure 6.37b of your text is incorrect.).



To derive the output resistance, we follow the same procedure as

above… with the same results. Therefore, for the CG amplifier:

$$R_{out} = [r_O + R_S(1 + g_m r_O)] \| R_D \cong R_D \quad if \quad r_O >> R_D .$$

To derive the input resistance, we need to use the figure above. Using KCL, the current through R_S may be expressed as (note that R_S is in parallel with v_{in} so it carries the same voltage and that the gate-to-source voltage is the same magnitude, but opposite polarity, as v_{in}):

$$i_{in} = \frac{v_{in}}{R_S} - g_m v_{gs} = \frac{v_{in}}{R_S} + g_m v_{in} = v_{in}\left(\frac{1}{R_S} + g_m\right). \qquad \text{(Equations 6.46 \& 6.47)}$$

Using this result, we can calculate the input resistance as

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{1/R_S + g_m} = R_S \| \frac{1}{g_m}. \qquad \text{(Equation 6.48)}$$

Using $v_{out} = -g_m v_{gs}(R_D||R_L) = g_m v_{in}(R_D||R_L||r_O)$, the voltage gain for the CG amplifier is given by:

$$A_V = \frac{g_m v_{in}(R_D \| R_L \| r_O)}{v_{in}} \cong g_m(R_D \| R_L) \quad if \quad r_O >> R_D, R_L . \qquad \text{(Equation 6.49)}$$

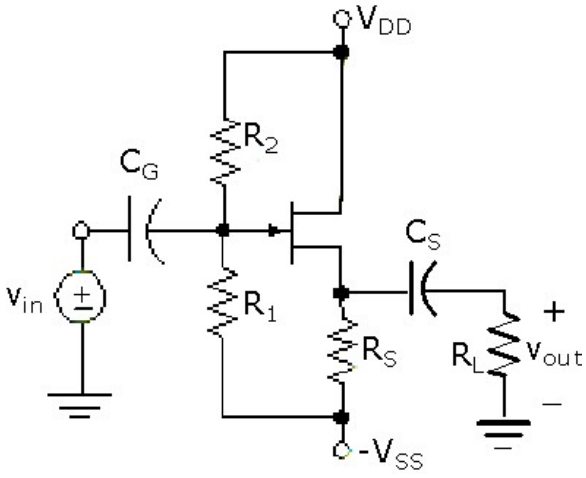
Note that the gain for the CG is the same as for the CS, without the negative sign. This means that the two configurations will provide the same voltage gain, but the CG output will be in phase with the input.

The current gain of the CG amplifier is given by:

$$A_i = \frac{(R_D \| R_L \| r_O)}{R_L} \frac{R_S}{R_S + 1/g_m} \cong \frac{R_D}{R_D + R_L} \frac{R_S}{R_S + 1/g_m} \quad if \quad r_O >> R_D, R_L \qquad \text{(Equation 6.50)}$$

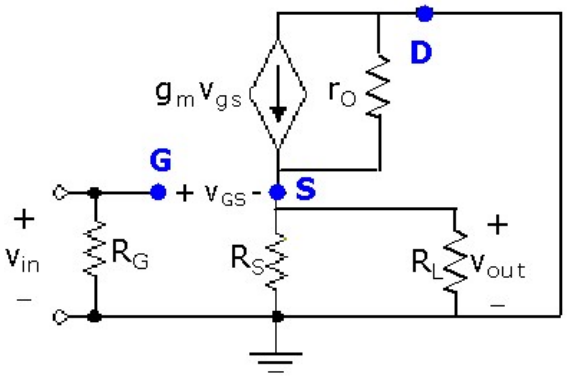
The CD (SF) Amplifier

Figure 6.39a (corrected and reproduced to the right) shows the schematic of a single-stage common drain (CD)/source follower (SF) circuit. As defined earlier, the ac input is applied at C_G, the ac output is taken at C_S and the drain is either connected to a dc voltage supply



or the drain resistor is bypassed with capacitor C_D (in this example the drain is connected to V_{DD} without C_D).

The ac small signal model for the CD (SF) amplifier is shown in Figure 6.39b and to the right.



Following the procedure used several times (this time we'll put a test voltage source in the source-ground leg and set $v_{in}=0$ so that $v_{gs}=-v_{test}$) an expression for the output resistance may be obtained:

$$i_{test} = \frac{v_{test}}{R_S} + g_m v_{test} = v_{test}\left(\frac{1}{R_S} + g_m\right), \text{ and}$$

$$R_{out} = \frac{v_{test}}{i_{test}} = \frac{1}{1/R_S + g_m} = R_S \parallel \frac{1}{g_m}. \qquad \text{(Equation 6.57)}$$

By inspection, the input resistance of the common drain amplifier is

$$R_{in} = R_G = R_1 \parallel R_2.$$

To solve for the voltage gain, we need expressions for v_{in} and v_{out} in terms of circuit components. By inspection, $v_{out}=g_m v_{gs}(R_S||R_L)$. To obtain the expression for v_{in}, write the KVL equation around the gate-source loop:

$$v_{in} = v_{gs} + (R_S \parallel R_L) g_m v_{gs} = v_{gs}[1 + g_m (R_S \parallel R_L)].$$

Calculating the voltage gain as the ratio of output voltage to input voltage:

$$A_V = \frac{g_m (R_S \parallel R_L)}{[1 + g_m (R_S \parallel R_L)]} = \frac{R_S \parallel R_L}{(R_S \parallel R_L) + 1/g_m}. \qquad \text{(Equation 6.54)}$$

And…finally, (the last one!) the current gain for the CD/SF configuration is:

$$A_i = \frac{R_G R_S}{(R_S + R_L)[(R_S \parallel R_L) + 1/g_m]}. \qquad \text{(Equation 6.55)}$$

The following table presents a summary of our discussions in this section. Note that these designations are with respect to the other FET configurations; for example, the CS is shown to have a high voltage gain, but it is still significantly lower than achievable with a BJT amplifier.

Amplifier Configuration	Z_{in}	Z_{out}	A_v	A_i
Ideal	∞	0	∞	∞
Common Source (CS)	High	High	High	High
Source Resistor (SR)	High	High	Medium	Medium
Common Gate (CG)	Low	Low	High	Low (~1)
Source Follower (SF)/ Common Drain (CD)	High	Low	Low (~1)	High