Section G2: Current Sources and Active Loads

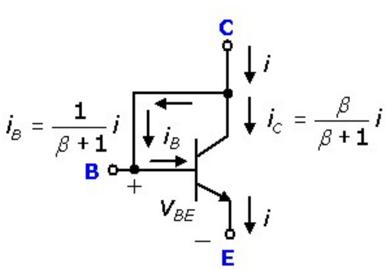
The transistor biasing techniques introduced in earlier sections are not suitable for the design of IC amplifiers since, even for a relatively simple multistage amplification system, many resistors and large capacitors are required. This is problematic for a couple of reasons, most importantly the cost of chip “real-estate” and fabrication concerns. However, fabrication of simple transistors has become cheap and easy, as well as providing the ability to have a large number of transistors with matched characteristics. Therefore, biasing in integrated circuit (IC) design is based on the use of transistors configured to act as constant current sources. On a multistage amplifier IC chip, a constant dc current source is generated at one location and is then reproduced at different locations for biasing the various amplification stages. The major advantages to this approach include:

- the requirement for resistors, coupling capacitors and bypass capacitors is removed; and
- the biasing of the multiple stages track each other in case of parameter changes, such as voltage supply or temperature fluctuations.

In this section, we will be looking at several methods of providing a constant dc current source for amplifier biasing using simple transistor configurations. Many of the circuits used to generate bias currents are also used for providing large resistances for IC applications. The active loads created in this manner, as well as the dc current sources, are small and easy to fabricate on IC chips.

Diode Connected Transistors

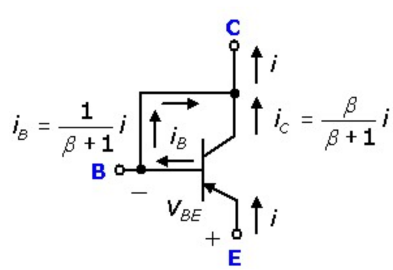
Before we get into current sources, let’s take a little bit to look at the details of the diode-connected transistor. In this configuration, the base and collector of the BJT are connected, or shorted as shown in the figures below for the npn (left) and pnp (right) transistors. The derivation of the currents on the figures is shown in the center.



Let $i_E = i$

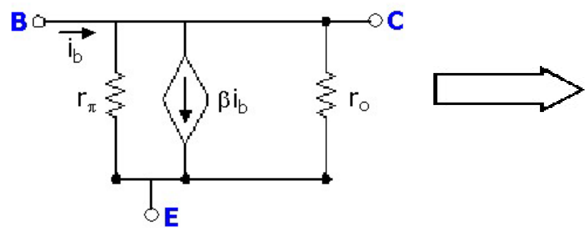
$$i_C = \alpha i_E = \frac{\beta}{\beta+1} i_E = \frac{\beta}{\beta+1} i$$

$$i_B = \frac{i_C}{\beta} = \frac{1}{\beta+1} i$$

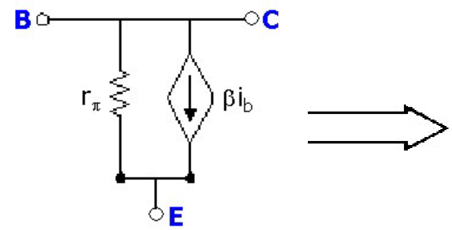


To illustrate the development of the simplified model for a diode-connected BJT, we're going to use the npn device. As usual, development for the pnp is directly analogous with current directions reversed and polarities switched.

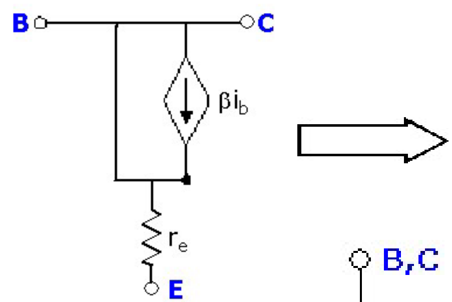
Starting with the usual small signal model, where the base and collector are shorted, we have:



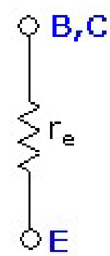
Assuming $r_\pi << r_o$, $r_\pi || r_o \approx r_\pi$ and the circuit is simplified to a single resistor in parallel with the dependent current source:



Now…reflecting r_π from the base circuit to the emitter circuit (recall that $r_\pi=(\beta+1)r_e$), we are left with a short in the base-emitter leg:



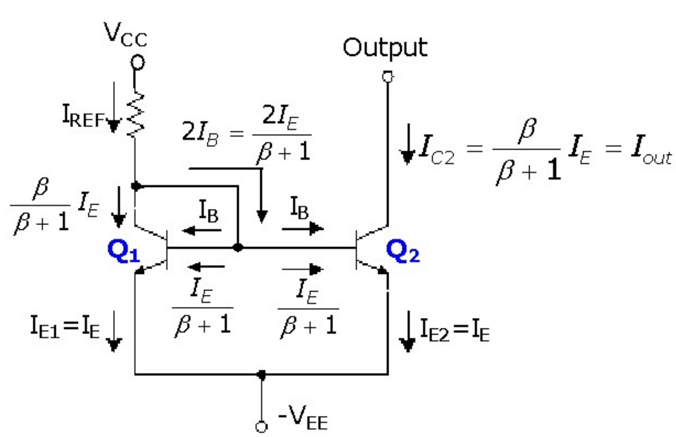
The dependent source is shorted out and we end up with a single resistance between the
base-collector terminal and the emitter terminal.



So, long story short. A diode-connected transistor may be replaced by a single resistor…pretty cool, huh?

A Simple Current Source (Current Mirror)

The most basic building block in the design of IC current sources, also known as the **current mirror**, is shown in the figure to the right (a modified version of Figure 5.27 in your text). The transistors, Q_1 and Q_2, are matched devices with their bases



and emitters tied together. The transistor designated Q_1 in the figure is connected as a diode by shorting its base and collector terminals.

A reference current, I_{REF}, is the input to the current mirror at the collector of the diode-connected transistor Q_1 and the output is taken from the collector of Q_2. Note: Q_2 must remain in the active (linear) region of operation by keeping its collector voltage higher than the base voltage at all times. It is important that the loading effect of any circuit fed by this current mirror should be inspected to ensure maintaining this mode of operation.

The key point to the analysis of the current mirror circuit is that the transistors are matched and have the same V_{BE}. Using this and examining the circuit above, the input current I_{REF} flows through Q_1 and sets up a voltage across Q_1. This voltage then appears across the base and emitter of Q_2 since the devices are connected in parallel. Assuming the assumption $I_C=I_E$ is valid ($\beta\approx\beta+1$), and using the fact that the transistors are matched, the emitter currents of Q_1 and Q_2 are the same and equal to I_{REF}. As long as Q_2 remains in the active region of operation, the output current, I_{out}, will also be approximately equal to I_{REF}.

If the effect of finite β is considered, the currents are as indicated in the figure above. This may lead to an output current that is not equal to the input reference current, since

$$I_{out} = \frac{\beta}{\beta+1} I_E \text{ and } I_{REF} = \frac{\beta+2}{\beta+1} I_E, \qquad \text{(Equations 5.59 \& 5.60)}$$

where the expression for I_{REF} is found by using KCL at the collector of Q_1. The current gain of the current mirror is

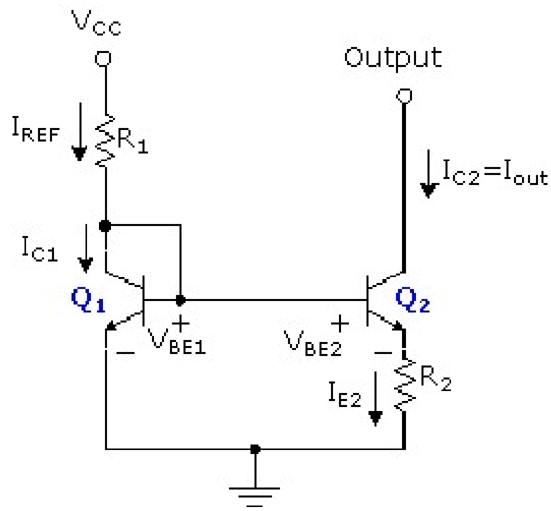
$$\frac{I_{out}}{I_{REF}} = \frac{\beta}{\beta+2},$$

which approaches unity for β very large. Another deviation of I_{out} from I_{REF} has to do with the Early effect. Since the V_{BE} of Q_2 is constant as determined by I_{REF}, the output resistance of Q_2 determines the dependence of I_{out}. This may be perceived as a disadvantage of this configuration – the output resistance of the current mirror (called R_{TH} in your text) is limited by the r_o of Q_2, or

$$r_o = \frac{V_A}{I_{out}} \approx \frac{V_A}{I_{REF}}.$$

Widlar Current Source

The Widlar current source differs from the basic current mirror in one important way – a resistor (R_2) is added to the emitter circuit of transistor Q_2. Since multistage amplifier systems often have high gain, bias currents must be small. Instead of the large resistors required to create small currents, the Widlar current source generates small constant currents using relatively small resistors. This allows considerable savings in chip real estate – which, as was mentioned before and will be mentioned often, is considered one of the ultimate goals in IC design.



The dc representation of Equation 4.10 is (assuming n=1)

$$I_C = I_o e^{\left(\frac{V_{BE}}{V_T}\right)}, \qquad \text{(Equation 4.10, Modified)}$$

where

I_o is the reverse saturation current

V_T is the thermal voltage ($kT/q \approx 26mV$ at room temperature)

Solving Equation 4.10 for V_{BE}, we get

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_O}\right).$$

Using this information, and neglecting base currents, we can express V_{BE1} and V_{BE2} in the circuit above as follows:

$$V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_O}\right) \cong V_T \ln\left(\frac{I_{REF}}{I_O}\right); \quad V_{BE2} = V_T \ln\left(\frac{I_{C2}}{I_O}\right) = V_T \ln\left(\frac{I_{out}}{I_O}\right).$$

Assuming we have matched devices, V_T and I_O are the same for Q_1 and Q_2. Subtracting V_{BE2} from V_{BE1}, and using the appropriate property of logarithms (i.e., lnA-lnB=ln(A/B)), we get

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{REF}}{I_{out}}\right).$$

Hang on, we're getting ready to use all this stuff!

Writing a KVL around the base loop of the two transistors,

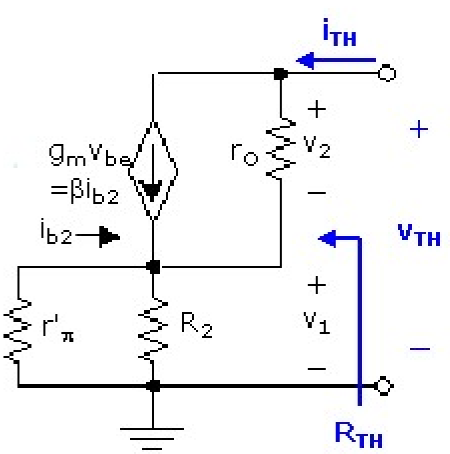
$$V_{BE1} = V_{BE2} + I_{E2}R_2;\ or\ V_{BE1} - V_{BE2} = I_{E2}R_2. \qquad \text{(Equation 5.61)}$$

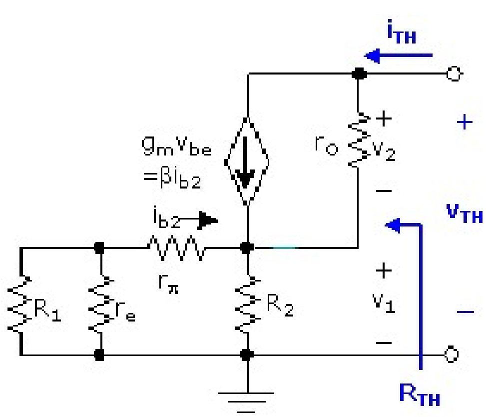
Here we go! Assuming that $I_{C2}=I_{E2}=I_{out}$, and using our expression for V_{BE1}-V_{BE2},

$$I_{out}R_2 = V_T \ln\left(\frac{I_{REF}}{I_{out}}\right). \qquad \text{(Equation 5.63, Modified)}$$

Since I_{REF} ($=I_{C1}$) is usually defined in design, Equation 5.63 can be solved for the required value of R_2.

Another improvement of the Widlar current source over the basic current mirror is the increased output resistance. The figure to the left below (Figure 5.29a) is the ac small signal model of the Widlar current source, and that to the right is a simplified version (Figure 5.29b), where $r'_\pi=(R_1||r_e)+r_\pi$. *Now, before you convince yourself that this cannot be right, remember that the small signal model of a diode connected BJT is simply r_e...*





Using the method of applying a test voltage v_{TH} and solving for the resulting current i_{TH} (or vice versa), we can solve for $R_{TH}=v_{TH}/i_{TH}$. Analyzing the simplified circuit (above right), we get the following definitions:

$$v_{TH} = v_1 + v_2$$
$$v_1 = -i_{b2} r'_\pi$$
$$v_2 = (i_{TH} - \beta i_{b2}) r_o \, . \qquad \text{(Equations 5.64 \& 5.65)}$$
$$i_{TH} = \beta i_{b2} + \frac{v_2}{r_o}$$

The equivalent output resistance is then given by:

$$R_{TH} = \frac{r_o(1 + \beta + r'_\pi / R_2) + r'_\pi}{1 + r'_\pi / R_2} \, . \qquad \text{(Equation 5.66)}$$

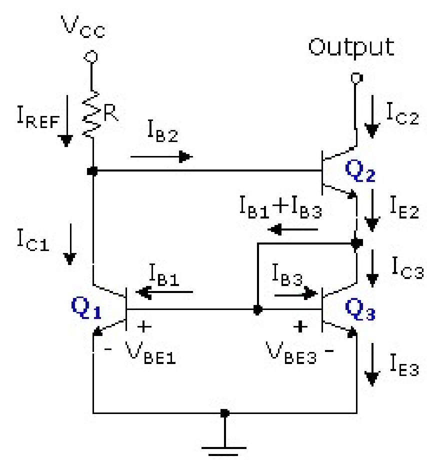
By making the assumption that r'_π is much larger than R_2, and using $r'_\pi = \beta V_T / I_{C2}$, the equivalent output resistance may be approximated by

$$R_{TH} = r_o\left(1 + \frac{I_{C2} R_2}{V_T}\right) = r_o\left(1 + \frac{I_{out} R_2}{V_T}\right). \qquad \text{(Equation 5.69)}$$

Note that the term $I_{out}R_2$ is the dc voltage drop across the resistor R_2 and the larger this voltage, the larger the output resistance.

Wilson Current Source

Another current source configuration that possesses increased output resistance is the Wilson current source. The increased r_o of the Wilson current source is due to the negative feedback provided by Q_3. This configuration uses three transistors as shown in Figure 5.30 of your text and as reproduced to the right.



Performing an analysis similar to the Widlar current source, we can derive an expression for the output resistance of the Wilson current source to be:

$$R_{TH} = \frac{\beta r_o}{2} = \frac{\beta V_A}{2 I_{C2}} \, . \qquad \text{(Equation 5.80)}$$

Writing a KCL equation at the emitter of Q_2:

$$I_{E2} = I_{C3} + I_{B1} + I_{B3}. \quad \text{(Equation 5.71)}$$

If all three transistors are matched $V_{BE1}=V_{BE2}=V_{BE3}$, $\beta_1=\beta_2=\beta_3$, $I_{B1}=I_{B3}$, and $I_{C1}=I_{C3}$. With this information and the relationship between base and collector currents ($I_B=I_C/\beta$), we can rewrite the expression for I_{E2} as

$$I_{E2} = I_{C3}\left(1+\frac{2}{\beta}\right). \quad \text{(Equation 5.73)}$$

Using $I_{C2}=\alpha I_{E2}=\beta I_{E2}/(\beta+1)$ and simplifying,

$$I_{C2} = \frac{I_{C3}(1+2/\beta)\beta}{\beta+1} = \frac{I_{C3}(\beta+2)}{(\beta+1)}. \quad \text{(Equation 5.75, Modified)}$$

Now, if we sum the currents at the base of Q_2,

$$I_{C1} = I_{C3} = I_{REF} - I_{B2} = I_{REF} - I_{C2}/\beta. \quad \text{(Equation 5.76, Modified)}$$

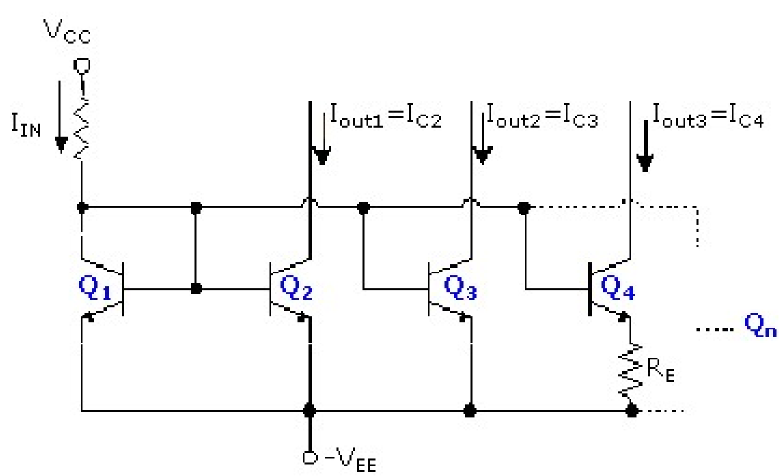
Substituting Equation 5.76 into Equation 5.75 and solving for I_{C2}, we get an expression for the output current (I_{C2}) in terms of the transistor parameter β and the input current, I_{REF}:

$$I_{C2} = \frac{\beta^2+2\beta}{\beta^2+2\beta+2} I_{REF} = \left(1-\frac{2}{\beta^2+2\beta+2}\right) I_{REF}. \quad \text{(Equation 5.78)}$$

For reasonable values of β, the second term will be negligible and $I_{C2}=I_{out}=I_{REF}$. Therefore, in addition to the increased output resistance, the Wilson configuration provides an output that is almost independent of the internal transistor characteristics…a very good thing!

Multiple Current Sources Using Current Mirrors

As mentioned earlier, a constant dc current may be generated at some point on a chip and reproduced at multiple other locations to bias the various amplifier stages on the IC. An example of such a circuit is shown to the right and is a



modified version of Figure 5.31 in your text. Note that Q_2 and Q_3 form a current mirror with transistor Q_1, while Q_4 is a Widlar current source because it has a resistor in the emitter leg. The amount of current delivered by this source can be determined by the size of this emitter resistor. Also, when using the Widlar circuit, the output current(s) may be different from the original reference current, I_{IN}.

However, there is a point of concern when using a multiple current source circuit. The effect of finite transistor β yields a cumulative effect of errors introduced by multiple base currents. This problem is easily overcome by restricting the number of outputs of the multiple current source and carefully selecting transistors with appropriate β.