Recall that the Class B amplifier was also referred to as a **push-pull** (or **complementary symmetry**) configuration, where one transistor is used to amplify the positive portion of the input signal and a second to amplify the negative portion of the input signal. A simplified Class B amplifier circuit is presented to the right (based on Figure 8.9 of your text). The circuit is powered by a **symmetrical** dc voltage source ($\pm V_{CC}$), with a **complementary** pair of transistors ($Q_1$ is an npn, while $Q_2$ is a pnp). These transistors are connected in such a way that both cannot conduct simultaneously:

- When the input voltage is zero, both transistors are cut off and the output voltage is zero.
- When the input voltage goes positive and is sufficiently large (approximately 0.7 V for silicon transistors), $Q_1$ turns on and conducts current from the $+V_{CC}$ supply to ground through the load resistance. $Q_1$ acts as an emitter-follower and $v_{out} = v_{in} - V_{BE1}$. During the positive half cycle of $v_{in}$, $Q_2$ remains cutoff.
- Similarly, when the input voltage goes negative and is less than approximately $-0.7$ V, $Q_2$ turns on and conducts current from ground to the $-V_{CC}$ supply through the load resistance. During the negative half of the input cycle, $Q_2$ acts as an emitter follower and $v_{out}$ follows $v_{in}$ ($v_{out} = v_{in} + V_{BE2}$) and $Q_1$ is cut off.

To summarize: the transistors in the Class B configuration are biased at zero current and are on (conduct current) only when an input signal has a magnitude greater than the turn-on voltage ($|V_{BE}| \approx 0.7V$ for Si BJTs). The Class B circuit has a combined **push-pull** effect on the load resistor – when $Q_1$ is on (when $v_{in}$ is sufficiently positive), it pushes (sources) current into the load and when $Q_2$ is on (when $v_{in}$ is sufficiently negative), it pulls (sinks) current from the load.

When the input signal is in the range that both transistors are off (approximately $-0.7V < v_{in}(t) < 0.7V$ for silicon BJTs), there exists a **dead band** where the output is zero for a nonzero input. This dead band results in the **crossover distortion** shown in
the figure to the right for the case of a sinusoidal input. The crossover
distortion is most obvious when the amplitude of the input signal is small
and contributes to the total harmonic distortion (THD) of the output signal.
An effective method for reducing crossover distortion involves the selection
of the bias points for transistors Q₁ and Q₂. Rather than designing for
conduction times of exactly one half cycle (Class B), the design is made for
transistor conduction times that are slightly longer than one half cycle (Class
AB).

Other important design considerations for complementary symmetry (Class
B and Class AB amplifiers) involve:

- Careful matching of the npn and pnp transistor electrical characteristics.
  Any asymmetry of the positive and negative portions of the output
  waveform also contributes to the THD of the output signal.
- Power
  - supplied to the load,
  - provided by the dc voltage source(s), and
  - dissipated in the transistors.

The remainder of our discussion in this section will analyze complementary
symmetry amplifiers that are operating in Class B or Class AB mode. Your
author notes that complementary symmetry amplifiers may also be used in
Class C operation, especially for high-efficiency, high-power radio frequency
(RF) amplifier applications.

**Complementary Symmetry Class B and Class AB Power Amplifiers**

The circuit for a typical push-pull power amplifier is shown to the right (Figure
8.11a of your text). In this figure:

- An npn transistor (Q₁) and a pnp
  transistor (Q₂) with symmetrical
electrical characteristics are each
  configured as an EF amplifier stage.
- Each amplifier stage has its own
  resistors to form the voltage divider
  that feeds the base; however, these
  resistances are symmetrical for the two
  EF amplifier stages (i.e.,
  \( R₁(Q₁) = R₁(Q₂) = R₁ \)
  and
  \( R₂(Q₁) = R₂(Q₂) = R₂ \). These resistors are
  selected so that the base-to-emitter voltages of both transistors (\( V_{BE1} \) and
  \( V_{BE2} \))
V_{BE2} \text{ place the Q-points at the boundary between cutoff and active mode.}

\text{dc isolation of the input signal and load is provided by capacitors } C_{in} \text{ and } C_1.

\text{A single dc power supply is used (} V_{CC} \text{). Note that the capacitor } C_1 \text{ serves an additional purpose in this circuit in that it acts as a power supply to } Q_2 \text{ when } Q_1 \text{ is not conducting. This is possible since the capacitor charges to a dc value of } V_{CC}/2 \text{ at the connection of the two emitters, for an effective dc source of } V_{CC}/2 \text{ for each EF amplifier stage.}

\text{If the Thevenin equivalent voltage (} V_{BB} \text{) resulting from the voltage divider in the circuit above is equal to } V_{BE}, \text{ the quiescent collector current is equal to zero and the amplifier is operating as Class B. However, if } V_{BB} > V_{BE}, I_{CQ} > 0 \text{ and the amplifier is operating as Class AB. The analysis of either EF stage (half of the total power amplifier circuit) mirrors the presentation of the EF (a.k.a. CC) configuration of Section D4, where } R_E \text{ is now zero and the dc source is } V_{CC}/2.

Another version of the Class AB amplifier is given in Figure 8.11d of your text and is reproduced to the right. In this version, the two } R_1 \text{ resistors have been replaced with a single variable resistor } R_X. \text{ } R_X \text{ is made larger than } 2R_1 \text{ to raise } I_{CQ} \text{ above zero, thereby compensating for distortion. If } R_X \text{ is chosen to be much smaller than } R_2, \text{ it may be neglected and the bases of the two transistors may be considered at the same potential. In this case, the equivalent base resistance of the circuit is}

\[ R_B = R_2 || R_2 = \frac{R_2}{2}. \]

As we mentioned above for the first circuit, analysis or design of the Class AB half-circuit proceeds as for an EF amplifier.

\textit{Complementary Symmetry Diode Compensated Power Amplifiers}

The circuit of Figure 8.12 (given to the right) shows a scheme for possible improvement in circuit operation with respect to thermal stabilization. The effects of the changes in the base-to-emitter voltage (} V_{BE} \text{) of a BJT with temperature variations may be reduced by
replacing the two $R_1$ resistors in the first circuit (Figure 8.11a) with diodes or diode connected BJTs. It is very important that the diodes have characteristics matched to those of the transistors used in the power amplifier and that they be mounted on the same heat sink. When using diode compensation, it is also necessary to know, or be able to estimate, the diode forward resistance $R_f$. Recall from our discussion of diodes (way back!) that the instantaneous slope of the diode forward characteristic curve is the inverse of the diode forward resistance. Estimates of $R_f$ may be determined as outlined in your text: the instantaneous values of voltage and current may be read from curves supplied by the manufacturer and $R_f$ is calculated by

$$R_f = \frac{\Delta V}{\Delta I} = \frac{V_2 - V_1}{I_2 - I_1},$$

where points 1 and 2 are close enough on the curve to approximate a straight line. Note that the value of $R_f$ depends upon the location on the curve and may vary greatly depending upon the value of the instantaneous forward current. However, your author states that the design of the amplifier is not highly dependent upon the value of $R_f$ and it is acceptable to use a fixed value.

It is also **extremely important** that the diode bias current be large enough to keep the diodes forward biased for all possible input voltages. The maximum negative peak current through the diode under ac operation must be less than the direct current bias. In other words, when the ac ($i_d$) and dc ($I_D$) portions of current through the diode are added together, the resultant current ($I_d$) should never go negative, or

$$i_d = I_D + i_d \geq 0; \quad \text{or} \quad I_D > |i_{dp}|,$$

(Equation 8.21, Modified)

where $i_{dp}$ is the peak value (positive or negative) of the ac component of the diode current. If this sum is negative, or $I_D < |i_{dp}|$, the diode would be reverse biased and significant distortion would result.

If the diodes are forward biased and matched, they may each be replaced with the general dc diode model of Section B4. The circuit to the right illustrates this strategy, where it is assumed that the diodes are forward biased. Note that this is extremely similar to the first circuit discussed in this section (Figure 8.11a).
The dc component of current through the diode may be calculated by

\[ I_D = \frac{(V_{CC}/2) - V_{BE}}{R_f + R_2} \approx \frac{(V_{CC}/2) - V_{BE}}{R_2}, \quad \text{(Equation 8.22)} \]

where the simplification was made by assuming \( R_f << R_2 \). Note that this is generally a valid assumption and illustrates why the instantaneous value of \( R_f \) is not absolutely critical in the design process.

The ac small signal midband circuit for the positive half cycle of the input signal is shown to the right. Recall that during the positive half cycle of the input, the npn transistor is conducting and the pnp transistor is cut off. Note that this schematic is based on Figure 8.13 of your text and, for now, we’re going to assume ideal capacitors that have zero reactance for the frequencies of interest. Also note that the emitter resistance \( r_e \) is omitted from the circuit since it is assumed to be very small when compared to other circuit resistors. By KCL at \( \text{a} \), the current through the diode is the sum of the base current and the current through \( R_2 \). In terms of peak values (indicated by the subscript p), this may be written as

\[ i_{dp} = i_{bp} + i_{R2p} = i_{bp} + \frac{v_{inp}}{R_2 + R_f} \approx i_{bp} + \frac{v_{outp}}{R_2}, \quad \text{(Equation 8.23)} \]

where the last equality is derived by assuming \( R_f << R_2 \) and that the voltage gain for the EF amplifier is unity \((A_V=1, \text{ or } v_{out}=v_{in})\). By equating the dc diode current \((I_D)\) to the peak value of the ac diode current \((i_{dp})\), we may find the limiting condition for operation in the forward biased diode region (Equation 8.21) as

\[ \frac{(V_{CC}/2) - V_{BE}}{R_2} = i_{bp} + \frac{v_{outp}}{R_2}. \quad \text{(Equation 8.24)} \]

From the small signal circuit above, the output voltage may be found by

\[ v_{out} = R_L(\beta + 1)i_b \approx R_L\beta i_b \quad \text{if} \quad \beta >> 1. \quad \text{(Equation 8.27)} \]
Solving the limiting condition in Equation 8.24 for $R_2$ and the expression of Equation 8.27 for $i_b$, the value of $R_2$ may be calculated by

$$R_2 = \frac{(V_{CC} / 2 - V_{BE} - v_{out})}{i_{bp}} = \frac{R_L \beta (V_{CC} / 2 - V_{BE} - v_{out})}{v_{out}}.$$  \hspace{1cm} (Equation 8.25)

Similarly, if $R_2$ is defined, the required value for the peak base current may be calculated by manipulating Equations 8.24 and 8.27:

$$i_{bp} = \frac{(V_{CC} / 2 - V_{BE} - v_{out})}{R_2} = \frac{(V_{CC} / 2 - V_{BE})}{R_2 + \beta R_L}.$$  \hspace{1cm} (Equation 8.25)

If we now “fold” the circuit above so that all grounds are at the same point, and reflect the load resistance up into the base circuit (using $\beta \gg 1$), we get the schematic to the right (based on Figure 8.14 of your text). By inspection, the input resistance is equal to

$$R_{in} = (R_f + R_2) || [R_f || (R_2 + \beta R_L)].$$  \hspace{1cm} (Equation 8.28)

The current gain may be derived from Figure 8.14 as

$$A_i = \frac{\beta i_b}{i_{in}} = \frac{\beta (R_f + R_2) R_2}{(2R_f + R_2 + R_2 || \beta R_L)(R_2 + \beta R_L)}.$$  \hspace{1cm} (Equation 8.30)

**Power Calculations for the Class B Amplifier**

Unlike the Class A amplifier that dissipates maximum power under quiescent conditions ($V_{CEQ}I_{CQ}$), the quiescent power dissipation of transistors in the Class B stage is zero since $I_{CQ}=0$. However, the power delivered by the source is still split between the transistor (average power over a half cycle) and the resistors of the bias circuitry, with the ac signal source providing an additional (but usually insignificant) amount of power. The various power relationships in the circuit are specified as follows:

- Neglecting the crossover distortion of the Class B amplifier, and assuming the gain of each EF stage is equal to one, we can see that the maximum current drawn from the dc supply during a half cycle is equal to $(V_{CC}/2)/R_L$. The power delivered to the transistors is equal to the source
voltage multiplied by the maximum collector current over the half-cycle of operation:

\[ P_{VCC} = \frac{V_{CC}^2}{2\pi R_L}. \]  (Equation 8.33)

The total dc power supplied to the Class B stage is the sum of the power to the transistors and the power to the bias and compensation circuitry:

\[ P_{VCC\ (total)} = \frac{V_{CC}^2}{2\pi R_L} + \frac{V_{CC}^2}{2(R_f + R_2)}. \]  (Equation 8.36)

Note: the above expression was derived for the diode compensated circuit, but still holds for the circuit of Figure 8.11a if \( R_f \) is replaced with \( R_1 \). Also, if \( R_C \) and/or \( R_E \) is included in the dc bias circuitry, appropriate modifications must be made to Equation 8.32.

Assuming a sinusoidal input, the maximum ac output power is

\[ P_{out\ (ac\ max)} = \frac{1}{2} \left( \frac{V_{CC} / 2}{R_L} \right)^2 R_L = \frac{1}{2} \left( \frac{(V_{CC} / 2)^2}{R_L} \right). \]  (Equation 8.35)

Neglecting the power dissipated by the bias circuitry, we calculate the efficiency of the Class B amplifier as the ratio of the ac output power to the power delivered to the transistors.

\[ \eta = \frac{P_{out\ (ac\ max)}}{P_{VCC}} \times 100 = \frac{\pi}{4} \times 100 = 78.5\%. \]  (Equation 8.38)

Therefore, the Class B amplifier provides a significant improvement in efficiency over the Class A configuration and is the output stage of choice when efficiency is an important design requirement.

To ensure a viable design, it is critical that the power rating of the transistor is sufficient. Maximizing Equation 8.37 with respect to collector current, we come up with the criteria for the maximum power of the transistor:
\[ P_{\text{max}} = \frac{V_{cc}^2}{4\pi^2 R_L}. \]  

(Equation 8.40)

In choosing a transistor for a design, it is extremely important that the power rating of the device is equal to or exceeds (smarter!) the maximum power calculated through Equation 8.40.