Section C8: Analysis and Design of Voltage Amplifier Bias Circuits

Analysis of a transistor amplifier circuit involves examining the dc bias conditions, determining the operating point, and examining ac operation using specified circuit components. In the design of a transistor amplifier, the situation is reversed. Depending on specifications or desired results, the challenge is to use all the stuff we’ve talked about to select circuit components to optimize performance.

Analysis Procedure

For any of the four basic configurations, amplifier analysis begins with known values of $R_1$, $R_2$, $V_{CC}$, $V_{BE}$, $R_E$, $R_C$, $R_{Load}$, and $\beta$. Your text begins the analysis procedure with the base side of the amplifier to “decouple” the equations as much as possible, but states that you may begin anywhere as long as you have as many independent equations as you have unknowns.

As discussed in the section on single-amplifier biasing, the first step is to develop the **Thevenin equivalent** for the base circuit:

\[
V_{BB} = V_{TH} = \frac{R_1V_{CC}}{R_1 + R_2} \\
R_B = R_{TH} = R_1 \parallel R_2 = \frac{R_1R_2}{R_1 + R_2}. \quad (\text{Equation 4.38 (also 4.22)})
\]

The base circuit conditions establishes the **quiescent collector current** to be

\[
I_{CQ} = \frac{V_{BB} - V_{BE}}{R_B/\beta + R_E}. \quad (\text{Equation 4.39 (also 4.24)})
\]

Equation 4.25 specifies the **dc load line** of the amplifier by establishing the axis intercept points $V_{CC}$ ($I_C=0$) and $I_{CC}$ ($V_{CE}=0$), where

\[
I_{CC} = \frac{V_{CC}}{R_E + R_C} = \frac{V_{CC}}{R_{dc}}.
\]

Under ac conditions, the load line changes since the equivalent circuit resistance changes when the bypass capacitors short some resistors and the coupling capacitor brings the load resistor into play (remember that dc
sources are shorts to ac). The **ac load line** has a slope with magnitude 1/R_{ac}, but it **must also pass through the Q-point** defined by the dc bias circuitry. The equation that defines the ac load line in point-slope form is given by

\[ I_C = \frac{-1}{R_{ac}} V_{CE} + \frac{V_{cc}'}{R_{ac}} \quad \text{or} \quad V_{CE} = V_{cc}' - I_C R_{ac} \]  

(Equation 4.45)

where \( I_{cc}' = \frac{V_{CEQ}}{R_{ac}} + I_{CQ} \).

To summarize:

<table>
<thead>
<tr>
<th>Configuration</th>
<th>R_{dc}</th>
<th>R_{ac}</th>
</tr>
</thead>
<tbody>
<tr>
<td>common-emitter</td>
<td>R_E + R_C</td>
<td>R_C \parallel R_{Load}</td>
</tr>
<tr>
<td>emitter-resistor</td>
<td>R_E + R_C</td>
<td>R_C \parallel R_{Load} + R_E</td>
</tr>
<tr>
<td>common-collector (with R_C)</td>
<td>R_E + R_C</td>
<td>R_E \parallel R_{Load}</td>
</tr>
<tr>
<td>common-collector (without R_C)</td>
<td>R_E</td>
<td>R_E \parallel R_{Load}</td>
</tr>
<tr>
<td>common-base</td>
<td>R_E + R_C</td>
<td>R_C \parallel R_{Load} + R_E \parallel R_{in}</td>
</tr>
</tbody>
</table>

The results of the above discussion are illustrated in Figure 4.17 (reproduced below).
To find the **maximum possible symmetrical output swing**, use the ac load line and see how far $i_C$ can vary from the Q-point before reaching the linear region boundaries (i.e., before $i_C$ enters the saturation or cutoff regions). Usually, the cutoff is assumed to be zero so

- if the Q-point is on the upper half of the ac load line, the maximum amplitude of the output current will be $I'_C - I_{CQ}$, or
- if the Q-point is on the lower half of the ac load line, the maximum amplitude of the output current will be $I_{CQ} - 0$.

Once the maximum amplitude of the output current has been determined, the maximum possible symmetric output swing is the total current swing multiplied by the effective load resistance, or

$$V_{out,\text{max}} = 2I_{C(\text{max peak})}R_{\text{Load, effective}}.$$  

where

<table>
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<tr>
<td>common-emitter</td>
<td>$R_C</td>
</tr>
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<td>$R_E</td>
</tr>
<tr>
<td>common-base</td>
<td>$R_C</td>
</tr>
</tbody>
</table>

**Design Procedure**

In analysis, we were given certain components that determined the Q-point and operational characteristics of the transistor amplifier. Now the shoe is on the other foot - we want to get certain operational or behavioral characteristics. To do this, we need to determine the circuit components that will give us an optimum Q-point and signal swing (beware that this may not always be a maximum possible output swing) by defining the ac and dc load lines.

**Just a little heads up from your author: sometimes it is not necessary to design an amplifier for maximum possible output swing. If the input signal is small and the desired gain is such that the output will never get near saturation and/or cutoff, it may be a waste of power to place the Q-point near the middle of the load line because of the dc power dissipated in the transistor. While this is definitely true, I, personally, have the habit of the 1/3 rule we talked about earlier. Many times there is no single way of doing something - this game turns out to be optimizing and you will**
develop your personal style (within reason, of course!) Hmm... the “rock and the hard place” quandary...

Anyway, to design a transistor amplifier, start at the collector-emitter side to define the load lines and the Q-point. For right now, we’re going to assume that \( R_C \) and \( R_E \) are given.

Please refer to Figure 4.17 in your text (reproduced above) and the analysis discussion for the following development. Your author begins the design process by defining \( I_{CQ} \) as a fraction of \( I'_CC \) through a parameter \( \delta \).

\[
I_{CQ} = \delta I'_CC, \text{ where } 0 < \delta < 1 \quad \text{(Equation 4.49: Modified)}
\]

Using the earlier definitions for \( I'_CC \) and \( V_{CEQ} \), \( I_{CQ} \) may be defined in terms of the known parameters \( V_{CC}, R_{ac}, R_{ac} \) and \( \delta \) (see above for \( R_{ac} \) and \( R_{dc} \) for the various amplifier configurations):

\[
I_{CQ} = \frac{V_{CC}}{R_{dc} + R_{ac} (1 - \delta)/\delta}. \quad \text{(Equation 5.53: Modified)}
\]

Once \( I_{CQ} \) is defined, your text offers several ways for calculating \( V_{CEQ} \):

\[
V_{CEQ} = \frac{(1 - \delta)}{\delta} I_{CQ} R_{ac} = V_{CC} - I_{CQ} R_{dc} = V'_{CC} (1 - \delta) \quad \text{(Equations 4.53 & 4.54)}
\]

Actually, the first and third options are essentially the same since your text defines \( V'_{CC} = I_{CQ} R_{ac}/\delta \) (Equation 4.55: Modified).

**Note:** If the design is for **maximum swing**, the Q-point needs to be in the middle of the load line so \( I_C \) can swing equally in both directions from \( I_{CQ} \). In this case, \( \delta=0.5 \) and the Q-point is located at the center of the load line at

\[
(V_{CEQ}, I_{CQ}) = \left( \frac{V_{CC}}{1 + (R_{dc}/R_{ac})}, \frac{V_{CC}}{R_{ac} + R_{dc}} \right). \quad \text{(Equation 6.68)}
\]

So, now that we’ve got the Q-point, we need to define the Thevenin equivalent circuit so we can define \( R_1 \) and \( R_2 \). To do this, we use the rule of thumb we discussed earlier to reduce the Q-point sensitivity, also known as a criteria for **bias stability**.
There are several techniques for accomplishing this, two of which are illustrated below. I don’t mind which you use, as long as I can figure out what you’re doing (i.e., document, document,..!)

Both of these techniques use the bias stability criteria \( R_E \gg R_B/\beta \) and the approximation given in Equation 4.61 (here, we’re assuming that \( \beta \) is given or we are advised of a nominal value):

\[
R_B = 0.1\beta R_E. \tag{Equation 4.61}
\]

**Technique 1** is presented by your author. Once the above approximation is made, the value of \( I_{CQ} \) is used to define \( V_{BB} \) (with \( V_{BEQ} = 0.7V \) for Si)

\[
V_{BB} = V_{BEQ} + I_{CQ}(1.1R_E). \tag{Equation 4.63}
\]

The expression for \( V_{BB} \) in Equation 4.38 is then rearranged to solve for \( R_1 \) and \( R_2 \):

\[
R_1 = \frac{R_B}{1-V_{BB}/V_{CC}} \quad \text{and} \quad R_2 = \frac{V_{CC}R_B}{V_{BB}}. \tag{Equation 4.64}
\]

**Technique 2** seems a little more natural to me, but once again, as long as I can figure out what you’re doing (and you are along the right track), we’re good to go!

As in technique 1, once \( R_B \) has been given a numeric value, we can solve for \( R_1 \) and \( R_2 \) by rearranging the parallel resistor relationship (remember that \( R_B = R_1 || R_2 \)):

\[
R_1 = \frac{R_2R_B}{R_2 - R_B} \quad \text{and} \quad R_2 = \frac{R_1R_B}{R_1 - R_B}.
\]

Finally, once \( R_1 \) and \( R_2 \) have been defined, \( V_{BB} \) can be calculated:

\[
V_{BB} = \frac{R_1V_{CC}}{R_1 + R_2}
\]

Remember, in this section of our studies, we are restricting ourselves to the case where \( R_C \) and \( R_E \) are defined for us. In the next
section (Chapter 5 material), when we discuss the amplifier configurations in more detail, this limitation will be lifted and we will design based on parameters such as the amplifier gain.

The maximum output voltage swing is still:

\[ V_{out,\text{max}} = 2I_{\text{C (max peak)}} R_{\text{Load-effective}}. \]

The maximum conversion efficiency (in percent) is given by Equation (4.37) and is repeated below:

\[ \eta_{\text{conversion}} = \frac{P_{\text{out (ac)}}}{P_{\text{in (dc)}}} \times 100. \]

Lastly (but certainly not least), is the maximum average power dissipated in the transistor:

\[ P_{\text{(transistor)}} = V_{CEQ} I_{CQ}. \]