Section B6: Rectification Using Semiconductor Diodes

 Practically, we live in an \textit{ac} world. However, many times a \textit{dc} signal is required and we have to have a way to convert between \textit{ac} and \textit{dc}. This requires restricting the original \textit{ac} signal that may alternate between positive and negative values to one that has values only on one side of the zero reference. The process of this conversion is called \textit{rectification} and may be classified as either half-wave rectification or full-wave rectification.

\textit{Half-Wave Rectification}

The simplest form of half-wave rectification is shown in Figure 3.30 in your text and is reproduced below in a more generic form. Part (a) of this modified figure corresponds to a simple two resistor circuit, where the relationship between the input and output voltages is defined by voltage division.

\begin{center}
\begin{align*}
\text{By voltage division: } v_o &= \frac{v_s R_L}{R_L + R} \\
\end{align*}
\end{center}

The circuit in part (b) actually illustrates the process of half-wave rectification. The rectifier uses the \textit{ideal diode current characteristics}; i.e., current flows when the diode is forward biased and no current flows when the diode is reverse biased. If we further assume that we’re dealing with an ideal diode (with $V_{on}=0.7\,\text{V}$), there is a simple 0.7 V drop across the diode in the forward bias region (that accounts for the turn-on voltage of a silicon diode). Using all this information, there are two distinct expressions for $v_o$ – a modified voltage divider relationship for forward bias, and a constant zero for reverse bias.
To keep the numbers straightforward in the example of Figure 3.30 in your text, a 100 V ac input is assumed with 90 V dropped across the load resistor due to the voltage divider (and by considering the 0.7 V drop across the diode as negligible). This figure and discussion are quite good for illustration purposes, but keep in mind that sometimes the 0.7 V may not be negligible!

Let’s look at the same circuit as the example in your text, and follow the same process, but change the input to $v_s = 1$ V.

$$v_{s(\text{max})} = 1V, \quad R = 10\Omega, \quad R_L = 90\Omega$$

*without diode*: $v_{o(\text{max})} = 0.9V$

*with diode*: $v_{o(\text{max})} = 0.27V$

Some difference huh? The shape of the curves will not change, and the input and output stay in phase for forward bias, but the 0.7V diode drop can no longer be considered negligible. That’s part of the art of this work, recognizing what can be neglected at what stage of the design/analysis and how any simplifications affect the final result.

No matter what the input and resistive divider consist of, the output waveform of the half-wave rectifier has the same characteristic – namely, it is a scaled version of the input sinusoid with the negative-going portion of...
the input chopped off if the diode is placed in the circuit as illustrated in Figure 3.30. Ask yourself, what would happen if the diode were flipped in the circuit? Think about it for a few minutes and then check out the answer in html or pdf.

Using a more generic version of Equation 3.41, where \( v_o \) is the scaled version of \( v_s \) that has a peak magnitude \( V_o \) (90 V in Equation 3.41 from Figure 3.30) and \( v_s \) is a sine wave of frequency \( \omega = 2\pi/T \), we get an average value for the output \( (v_o, avg) \), measured across the load resistor, of:

\[
v_{o,avg} = \frac{1}{T} \int_0^T v_o(t)dt = \frac{1}{T} \int_0^{T/2} V_o \sin \frac{2\pi t}{T} dt + \frac{1}{T} \int_{T/2}^T 0dt = \frac{V_o}{\pi} + 0 \approx 0.318V_o
\]

(Hmmm... this illustrates that the half-wave rectifier circuit we’ve been talking about is not very efficient... to the tune of about 31.8% of the peak output voltage being available for output power. It’s simple, it’s cheap, it’s easy, and with the proper filtering (to be discussed later) it can be used to create an almost constant dc output, but we lose the input energy over a complete half cycle (when it’s chopped off). If there was a way to transfer the input energy to the output over both half cycles, we would be able to increase output power.

**Surprise, surprise... there is, and this is a nice segue into the introduction of...**

**Full-Wave Rectification**

The full-wave rectifier is somewhat more complicated in any of its versions, but it has the major advantage that energy is transferred from the input to the output over both halves of the input cycle. This provides twice the average output voltage as the half-wave rectifier, or 63.6% of the peak output voltage. (Note: This can be shown mathematically by integrating over a full cycle in Equation 3.41 or, equivalently (for a sinusoid with zero offset or other symmetric signal), doubling the result over a half-cycle.) Regardless of the full-wave rectifier implementation, the input and output characteristics are illustrated below in terms of peak magnitudes \( V_s \) and \( V_o \):
So, how do we get here? Your text illustrates two common full-wave rectifier circuits and their outputs in Figures 3.31 through 3.33.

Figure 3.31 shows the circuit of a **transformer implementation of a full-wave rectifier**. The 100Vrms ac input is stepped up by the 1:2 transformer (for 200 Vrms ac on the secondary coil), which is then split in half by placing a ground tap in the center of the secondary. This effectively creates **two** 100Vrms ac input signals and allows for full-wave rectification. Figure 3.31 is reproduced below, with the paths indicated for

- A positive-going input \( v_s(t) \geq 0 \). Diode \( D_2 \) is reverse biased (“off”), \( D_1 \) is forward biased (“on”), and the current flows through \( R_L \) to create \( v_o \) with the polarity shown.
- A negative-going input \( v_s(t) \leq 0 \). Diode \( D_1 \) is reverse biased (“off”), \( D_2 \) is forward biased (“on”), and the current flows through \( R_L \) to create \( v_o \) ... still with the polarity shown.

Figures 3.32 and 3.33 show the circuit and output of a full-wave bridge rectifier. These two figures have been combined and reproduced below, with paths indicated for
A positive-going input \( v_s(t) > 0 \). Diodes D_2 and D_3 are reverse biased ("off"), diodes D_1 and D_4 are forward biased ("on"), and the current flows through \( R_L \) to create \( v_o \) with the polarity shown.

A negative-going input \( v_s(t) \leq 0 \). Diodes D_1 and D_4 are reverse biased ("off"), diodes D_2 and D_3 are forward biased ("on"), and the current flows through \( R_L \) to create \( v_o \) ... still with the polarity shown.

**NOTE:** Remember that determination of whether a diode is forward or reverse biased has to do with the potential across it. For example, the diode D_3 is reverse biased for the positive-going input case because the “bar” (cathode) of the diode is at a higher potential than the “tail” (anode).

There is a practical problem to the bridge rectifier as illustrated above. A **ground loop** may be formed if one of the source terminals is grounded and one of the terminals of the load resistor is also grounded. Prove to yourself that this situation would short out one of the diodes and destroy the rectification capacity of the circuit. To overcome this problem, a transformer is added to the circuit to isolate the source ground and load resistor ground.

This is as deep as we’re going to get into rectification. So far, we’ve succeeded in turning each period of an ac sinusoid into either a “single-hump and zero” (half-wave rectified) or “double-hump” (full-wave rectified) signal. Turning these **pulsating dc voltages** (as your text calls them) into an acceptable dc signal requires **filtering** which, not surprisingly, is the topic of the next section.