Due 12/9/2009

1. Using Design Vision, synthesize the FPU for lowest area. Report area, power dissipation and clock period – this is RTL-A.
2. Using Design Vision, synthesize the FPU for lowest power-delay. Report area, power dissipation and clock period – this is RTL-B.
3. Run Encounter on RTL-A with clock skew 100ps. Report area, power dissipation and clock period from Encounter – this is Layout-1.
4. Run Encounter on RTL-B with clock skew 100ps. Report area, power dissipation and clock period from Encounter – this is Layout-2.
5. For Layouts 1 and 2, report area, power dissipation and clock period from Encounter, with 2 different power/ground designs per layout.
6. Use RC extractor on all layouts. **Generate SPICE Netlists from the extracted LAYOUTs for the Clock Net** for all layouts. These Spice netlists should be in your report along with the corresponding circuit diagrams.
7. **Simulate the Clock Nets for (a) Power Dissipation and (b) Skew Distribution.**
8. **Derive the R,C parameters for the equivalent source CRC PI circuits and the RC sink circuits. Draw these circuits.**