Circuit Extraction and DRC

After detailed routing is complete, the exact length and position of each interconnect for every net is known. Now the parasitic capacitance and resistance associated with each interconnect, via, and contact can be calculated. This data is generated by a circuit-extraction tool in one of the formats described next. It is important to extract the parasitic values that will be on the silicon wafer. The mask data or CIF widths and dimensions that are drawn in the logic cells are not necessarily the same as the final silicon dimensions. Normally mask dimensions are altered from drawn values to allow for process bias or other effects that occur during the transfer of the pattern from mask to silicon. Since this is a problem that is dealt with by the ASIC vendor and not the design software vendor, ASIC designers normally have to ask very carefully about the details of this problem.

[Table 17.2](http://www10.edacafe.com/book/ASIC/CH17/CH17.4.php%22%20%5Cl%20%2219399) shows values for the parasitic capacitances for a typical 1 m m CMOS process. Notice that the fringing capacitance is greater than the parallel-plate (area) capacitance for all layers except poly. Next, we shall describe how the parasitic information is passed between tools.

**17.4.1** **SPF, RSPF, and DSPF**

The standard parasitic format ( SPF ) (developed by Cadence [ 1990], now in the hands of OVI) describes interconnect delay and loading due to parasitic resistance and capacitance. There are three different forms of SPF: two of them ( regular SPF and reduced SPF ) contain the same information, but in different formats, and model the behavior of interconnect; the third form of SPF ( detailed SPF ) describes the actual parasitic resistance and capacitance components of a net. [Figure 17.22](http://www10.edacafe.com/book/ASIC/CH17/CH17.4.php#23689) shows the different types of simplified models that regular and reduced SPF support. The load at the output of gate A is represented by one of three models: lumped-C, lumped-RC, or PI segment. The pin-to-pin delays are modeled by RC delays. You can represent the pin-to-pin interconnect delay by an ideal voltage source, V(A\_1) in this case, driving an RC network attached to each input pin. The actual pin-to-pin delays may not be calculated this way, however.

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| TABLE 17.2  Parasitic capacitances for a typical 1 m m ( l = 0.5 m m) three-level metal CMOS process. [1](http://www10.edacafe.com/book/ASIC/CH17/CH17.4.php#pgfId=76953)  |
| Element  | Area / fF m m –2  | Fringing / fF m m –1  |
| poly (over gate oxide) to substrate | 1.73 | NA [2](http://www10.edacafe.com/book/ASIC/CH17/CH17.4.php#pgfId=76971)  |
| poly (over field oxide) to substrate  | 0.058 | 0.043 |
| m1 to diffusion or poly | 0.055 | 0.049 |
| m1 to substrate | 0.031 | 0.044 |
| m2 to diffusion | 0.019 | 0.038 |
| m2 to substrate | 0.015 | 0.035 |
| m2 to poly | 0.022 | 0.040 |
| m2 to m1 | 0.035 | 0.046 |
| m3 to diffusion | 0.011 | 0.034 |
| m3 to substrate | 0.010 | 0.033 |
| m3 to poly | 0.012 | 0.034 |
| m3 to m1 | 0.016 | 0.039 |
| m3 to m2 | 0.035 | 0.049 |
| n+ junction (at 0V bias) | 0.36 | NA |
| p+ junction (at 0V bias) | 0.46 | NA |

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| http://www10.edacafe.com/book/ASIC/CH17/CH17-22.gif  |
| FIGURE 17.22  The regular and reduced standard parasitic format (SPF) models for interconnect. (a) An example of an interconnect network with fanout. The driving-point admittance of the interconnect network is Y ( s ). (b) The SPF model of the interconnect. (c) The lumped-capacitance interconnect model. (d) The lumped-RC interconnect model. (e) The PI segment interconnect model (notice the capacitor nearest the output node is labeled C 2 rather than C 1 ). The values of C , R , C 1 , and C 2 are calculated so that Y 1 ( s ), Y 2 ( s ), and Y 3 ( s ) are the first-, second-, and third-order Taylor-series approximations to Y ( s ).  |

The key features of regular and reduced SPF are as follows:

* The loading effect of a net as seen by the driving gate is represented by choosing one of three different RC networks: lumped-C, lumped-RC, or PI segment (selected when generating the SPF) [ O’Brien and Savarino, 1989].
* The pin-to-pin delays of each path in the net are modeled by a simple RC delay (one for each path). This can be the Elmore constant for each path (see [Section 17.1.2](http://www10.edacafe.com/book/ASIC/CH17/CH17.1.php#30196) ), but it need not be.

Here is an example regular SPF file for just one net that uses the PI segment model shown in [Figure 17.22](http://www10.edacafe.com/book/ASIC/CH17/CH17.4.php#23689) (e):

#Design Name : EXAMPLE1

#Date : 6 August 1995

#Time : 12:00:00

#Resistance Units : 1 ohms

#Capacitance Units : 1 pico farads

#Syntax :

#N <netName>

#C <capVal>

# F <from CompName> <fromPinName>

# GC <conductance>

# |

# REQ <res>

# GRC <conductance>

# T <toCompName> <toPinName> RC <rcConstant> A <value>

# |

# RPI <res>

# C1 <cap>

# C2 <cap>

# GPI <conductance>

# T <toCompName> <toPinName> RC <rcConstant> A <value>

# TIMING.ADMITTANCE.MODEL = PI

# TIMING.CAPACITANCE.MODEL = PP

N CLOCK

C 3.66

F ROOT Z

RPI 8.85

C1 2.49

C2 1.17

GPI = 0.0

T DF1 G RC 22.20

T DF2 G RC 13.05

This file describes the following:

* The preamble contains the file format.
* This representation uses the PI segment model ( [Figure 17.22](http://www10.edacafe.com/book/ASIC/CH17/CH17.4.php#23689) e).
* This net uses pin-to-pin timing.
* The driving gate of this net is ROOT and the output pin name is Z .
* The PI segment elements have values: C1 = 2.49 pF, C2 = 1.17 pF, RPI = 8.85 W . Notice the order of C1 and C2 in [Figure 17.22](http://www10.edacafe.com/book/ASIC/CH17/CH17.4.php#23689) (e). The element GPI is not normally used in SPF files.
* The delay from output pin Z of ROOT to input pin G of DF1 is 22.20 ns.
* The delay from pin Z of ROOT to pin G of DF2 is 13.05 ns.

The reduced SPF ( RSPF) contains the same information as regular SPF, but uses the SPICE format. Here is an example RSPF file that corresponds to the previous regular SPF example:

\* Design Name : EXAMPLE1

\* Date : 6 August 1995

\* Time : 12:00:00

\* Resistance Units : 1 ohms

\* Capacitance Units : 1 pico farads

\*| RSPF 1.0

\*| DELIMITER "\_"

.SUBCKT EXAMPLE1 OUT IN

\*| GROUND\_NET VSS

\* TIMING.CAPACITANCE.MODEL = PP

\*|NET CLOCK 3.66PF

\*|DRIVER ROOT\_Z ROOT Z

\*|S (ROOT\_Z\_OUTP1 0.0 0.0)

R2 ROOT\_Z ROOT\_Z\_OUTP1 8.85

C1 ROOT\_Z\_OUTP1 VSS 2.49PF

C2 ROOT\_Z VSS 1.17PF

\*|LOAD DF2\_G DF1 G

\*|S (DF1\_G\_INP1 0.0 0.0)

E1 DF1\_G\_INP1 VSS ROOT\_Z VSS 1.0

R3 DF1\_G\_INP1 DF1\_G 22.20

C3 DF1\_G VSS 1.0PF

\*|LOAD DF2\_G DF2 G

\*|S (DF2\_G\_INP1 0.0 0.0)

E2 DF2\_G\_INP1 VSS ROOT\_Z VSS 1.0

R4 DF2\_G\_INP1 DF2\_G 13.05

C4 DF2\_G VSS 1.0PF

\*Instance Section

XDF1 DF1\_Q DF1\_QN DF1\_D DF1\_G DF1\_CD DF1\_VDD DF1\_VSS DFF3

XDF2 DF2\_Q DF2\_QN DF2\_D DF2\_G DF2\_CD DF2\_VDD DF2\_VSS DFF3

XROOT ROOT\_Z ROOT\_A ROOT\_VDD ROOT\_VSS BUF

.ENDS

.END

This file has the following features:

* The PI segment elements ( C1 , C2 , and R2 ) have the same values as the previous example.
* The pin-to-pin delays are modeled at each of the gate inputs with a capacitor of value 1 pF ( C3 and C4 here) and a resistor ( R3 and R4 ) adjusted to give the correct RC delay. Since the load on the output gate is modeled by the PI segment it does not matter what value of capacitance is chosen here.
* The RC elements at the gate inputs are driven by ideal voltage sources ( E1 and E2 ) that are equal to the voltage at the output of the driving gate.

The detailed SPF ( DSPF) shows the resistance and capacitance of each segment in a net, again in a SPICE format. There are no models or assumptions on calculating the net delays in this format. Here is an example DSPF file that describes the interconnect shown in [Figure 17.23](http://www10.edacafe.com/book/ASIC/CH17/CH17.4.php#13082) (a):

.SUBCKT BUFFER OUT IN

\* Net Section

\*|GROUND\_NET VSS

\*|NET IN 3.8E-01PF

\*|P (IN I 0.0 0.0 5.0)

\*|I (INV1:A INV A I 0.0 10.0 5.0)

C1 IN VSS 1.1E-01PF

C2 INV1:A VSS 2.7E-01PF

R1 IN INV1:A 1.7E00

\*|NET OUT 1.54E-01PF

\*|S (OUT:1 30.0 10.0)

\*|P (OUT O 0.0 30.0 0.0)

\*|I (INV:OUT INV1 OUT O 0.0 20.0 10.0)

C3 INV1:OUT VSS 1.4E-01PF

C4 OUT:1 VSS 6.3E-03PF

C5 OUT VSS 7.7E-03PF

R2 INV1:OUT OUT:1 3.11E00

R3 OUT:1 OUT 3.03E00

\*Instance Section

XINV1 INV1:A INV1:OUT INV

.ENDS

The nonstandard SPICE statements in DSPF are comments that start with '\*|' and have the following formats:

\*|I(InstancePinName InstanceName PinName PinType PinCap X Y)

\*|P(PinName PinType PinCap X Y)

\*|NET NetName NetCap

\*|S(SubNodeName X Y)

\*|GROUND\_NET NetName

[Figure 17.23](http://www10.edacafe.com/book/ASIC/CH17/CH17.4.php%22%20%5Cl%20%2213082) (b) illustrates the meanings of the DSPF terms: InstancePinName , InstanceName , PinName , NetName , and SubNodeName . The PinType is I (for IN) or O (the letter 'O', not zero, for OUT). The NetCap is the total capacitance on each net. Thus for net IN, the net capacitance is

0.38 pF = C1 + C2 = 0.11 pF + 0.27 pF.

This particular file does not use the pin capacitances, PinCap . Since the DSPF represents every interconnect segment, DSPF files can be very large in size (hundreds of megabytes).

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| http://www10.edacafe.com/book/ASIC/CH17/CH17-23.gif  |
| FIGURE 17.23  The detailed standard parasitic format (DSPF) for interconnect representation. (a) An example network with two m2 paths connected to a logic cell, INV1. The grid shows the coordinates. (b) The equivalent DSPF circuit corresponding to the DSPF file in the text. |